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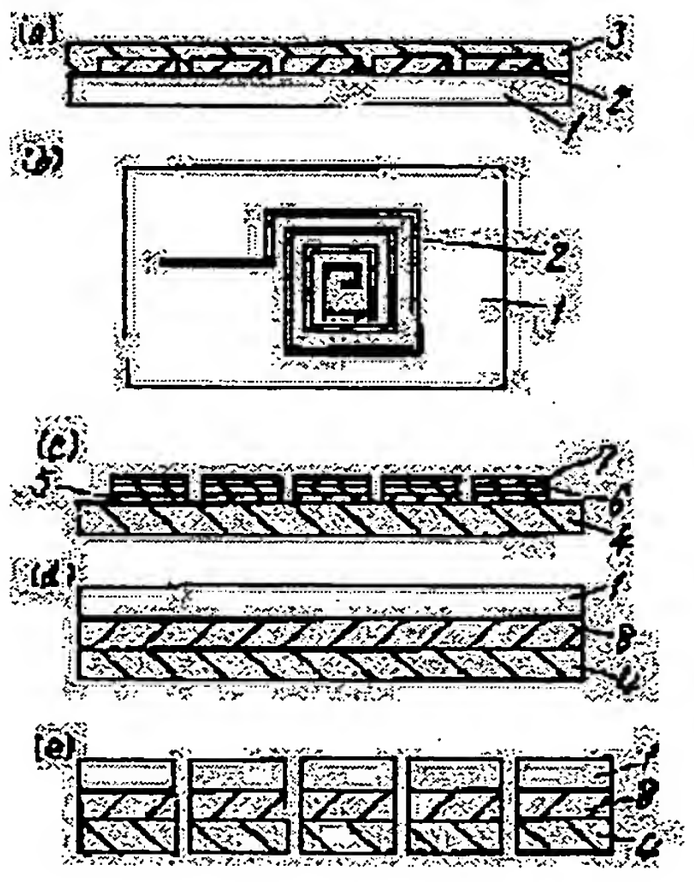
## (54) MANUFACTURE OF SOLID-STATE COMPOSITE PART

(57)Abstract:
PROBLEM TO BE SOLVED: To realize a manufacturing method of a small-sized solid-state composite part excellent in dimensional precision and reliability.
SOLUTION: A first unbaked ceramic substrate and a second unbaked ceramic substrate are baked, and a first ceramic substrate 1 and a second ceramic substrate 4 are formed. An inductor electrode 2 as an inductor conductor pattern layer is formed on the first substrate 1. A ferrite layer 3 as a magnetic paste layer is formed on the electrode 2, and an inductor layer is formed. A capacitor layer composed of a capacitor lower electrode 5, a capacitor upper electrode 7 and a dielectric layer 6 is formed as a capacitor conductor pattern layer on the second substrate 4. An adhesive glass layer 8 as a glass paste layer is spread on at least one out of the first and second ceramic substrates. The substrates are laminated and a laminate is formed. A baked body is formed by baking the laminate, and outer electrodes are formed on the baked body.



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## CLAIMS

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[Claim(s)]
[Claim 1] While forming an inductor conductor pattern layer on the whole surface of the 1st ceramic substrate The 1st process which forms a magnetic paste layer on said inductor conductor pattern layer, and forms the 1st substrate with an inductor layer, The 2nd process which forms the capacitor conductor pattern layer which intervened the dielectric layer on the whole surface of the 2nd ceramic substrate, and forms the 2nd substrate with a capacitor layer, While forming a glass paste layer at least in one side by the side of the whole surface of said 1st substrate, or the whole surface of said 2nd substrate The 3rd process which said the 1st substrate and said 2nd substrate are made to rival mutually through said glass paste layer, and forms tension coalesce, It has the 4th process which calcinates said tension coalesce and forms a baking object, and the 5th process which forms an external electrode in said baking object. The manufacture approach of solid-state composite part of having established the process which calcinates the 1st non-calcinated ceramic substrate and the 2nd non-calcinated ceramic substrate, and forms the 1st ceramic substrate and 2nd ceramic substrate before said 1st process.
[Claim 2] The process which the inductor conductor pattern layer of the 1st process fills up with a conductive paste the pattern slot established in the front face of the intaglio which consists of a flexible resin substrate, and is dried, The process made to rival, heating and pressurizing said intaglio and whole surface of the 1st ceramic substrate, The manufacture approach of solid-state composite part according to claim 1 of having the process which exfoliates said intaglio from said 1st ceramic substrate, and imprints said conductive paste on said 1st ceramic substrate, and the process which calcinates said 1st ceramic substrate.
[Claim 3] The manufacture approach of solid-state composite part according to claim 1 of having established the process which forms the interlayer of a glass paste layer between the 2nd ceramic substrate and a capacitor layer in the 2nd process.
[Claim 4] The manufacture approach of the solid-state composite part according to claim 3 which made the quality of the material of a glass paste layer the quality of the material with the glass frit which consists of any one of hoe silicic acid, a hoe lead silicate, a hoe calcium silicate, hoe aluminum silicate, and the hoe silicic acid titanium, its mixture, or its compound.
[Claim 5] The manufacture approach of solid-state composite part according to claim 1 of having established the process which carries out a debinder in the 3rd process after forming a glass paste layer.
[Claim 6] The manufacture approach of solid-state composite part according to claim 1 of having established the process which forms baking ****** before the 4th process so that the process which forms a silver electrode in said through tube while forming two or more through tubes in the 2nd ceramic substrate might be established, a baking object might be divided after the 4th process at the piece of an individual and said silver electrode might express on a side face, and having established the process formed in an external electrode with said silver electrode in the 5th process.
[Claim 7] The manufacture approach of solid-state composite part according to claim 1 of having established the process which divides a baking object into the piece of an individual, and forms baking ****** after the 4th process.
[Claim 8] The manufacture approach of solid-state composite part according to claim 1 of having established the process which carries out grinding of either [ at least ] the 1st ceramic substrate or the 2nd ceramic substrate, and makes thin one [ at least ] substrate thickness of the 1st ceramic substrate or the 2nd ceramic substrate after the 4th process.
[Claim 9] The 1st ceramic substrate and 2nd ceramic substrate are the manufacture approach of the solid-state composite part according to claim 1 which made the coefficient of thermal expansion equivalent mutually.
[Claim 10] The manufacture approach of the solid-state composite part according to claim 9 which made the quality of the material of the 1st ceramic substrate the quality of the material with a ferrite, and made the quality of the material of the 2nd ceramic substrate the quality of the material with forsterite.
[Claim 11] The manufacture approach of the solid-state composite part according to claim 1 which made area of a

capacitor conductor pattern layer larger than the area of a dielectric layer.
[Claim 12] The manufacture approach of the solid-state composite part according to claim 1 which made the quality of the material of a capacitor conductor pattern layer the quality of the material with the glass frit which consists of any one of hoe silicic acid, a hoe lead silicate, a hoe calcium silicate, hoe aluminum silicate, and the hoe silicic acid titanium, its mixture, or its compound.
[Claim 13] The manufacture approach of solid-state composite part according to claim 1 of having established the process which forms a two or more layers inductor conductor pattern layer.
[Claim 14] an inductor conductor pattern layer -- a line -- the conductor was made spiral -- spiral -- a conductor -- the section -- having -- said -- spiral -- a conductor -- said line of the section -- the manufacture approach of solid-state composite part according to claim 1 that the conductor exceeded 0.3 for the conductor thickness ratio to a conductor width.
[Claim 15] an inductor conductor pattern layer -- a line -- the conductor was made spiral -- spiral -- a conductor -- it has at least two sections and adjoins -- said -- spiral -- a conductor -- the manufacture approach of solid-state composite part according to claim 1 of having established the process which forms a non-magnetic material on ******.
[Claim 16] an inductor conductor pattern layer -- a line -- the conductor was made spiral -- spiral -- a conductor -- it has at least two sections and adjoins -- said -- spiral -- a conductor -- while forming a non-magnetic material on ****** -- said -- spiral -- a conductor -- the manufacture approach of solid-state composite part according to claim 1 of having established the process which forms a slot in the 1st ceramic substrate on ******, and forms said non-magnetic material also in said slot.
[Claim 17] an inductor conductor pattern layer -- a line -- the conductor was made spiral -- spiral -- a conductor -- the section and a line -- the shape of a ring which made the conductor the shape of a ring -- a conductor -- the section -- having -- said -- spiral -- a conductor -- the outside of the section -- the shape of said ring -- a conductor -- the manufacture approach of solid-state composite part according to claim 1 of having established the process which forms the section.
[Claim 18] an inductor conductor pattern layer -- a line -- the conductor was made spiral -- spiral -- a conductor -- the section and a line -- the shape of a ring which made the conductor the shape of a ring -- a conductor -- the section -- having -- said -- spiral -- a conductor -- the outside of the section -- the shape of said ring -- a conductor -- while forming the section -- the shape of said ring -- a conductor -- the manufacture approach of solid-state composite part according to claim 1 of having established the process which forms the section into a magnetic paste layer.
[Claim 19] the shape of a ring -- a conductor -- the manufacture approach of solid-state composite part according to claim 17 of having established the process which carries out ground connection of the section.
[Claim 20] spiral -- a conductor -- the shape of the section and a ring -- a conductor -- the manufacture approach of solid-state composite part according to claim 17 of having established the process which forms the section on the same flat surface at coincidence.

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## DETAILED DESCRIPTION

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[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the manufacture approach of the solid-state composite part of the chip mold which the inductor, the capacitor, etc. compounded.
[0002]
[Description of the Prior Art] In recent years, small and lightweight-ization are progressing, Semi-conductor LSI, a chip, etc. have the demand of a miniaturization also with a high frequency-related magnetic device in this, the demand of a miniaturization of the capacitor which used the dielectric of a thick film increases, and the approach of making a dielectric and an inductor unification and making them small into one device, etc. has been developed.
[0003] the capacitor formation approach of having attained the miniaturization -- JP,2-54647,B -- setting -- a nonmagnetic insulator layer and the electrode for capacitors -- a conductor -- crosswise lamination -- carrying out -- the nonmagnetic insulator layer of the still more nearly same quality of the material on it, and the object for coils -- crosswise lamination of the conductor is carried out and the method of really calcinating these, compound-izing an inductor and a capacitor, and attaining a miniaturization is introduced. Moreover, as the manufacture approach of simpler solid-state composite part, a magnetic-substance sheet and a dielectric sheet are calcinated and the method of carrying out lamination unification by the interlayer is introduced as indicated by JP,57-193019,A.
[0004]
[Problem(s) to be Solved by the Invention] By the above-mentioned conventional approach, in order to really calcinate an inductor and a capacitor, a magnetic-substance sheet and a dielectric sheet need to use low-temperature-sintering material, and it is hard to aim at improvement in a property. Moreover, from the difference in the coefficient of thermal expansion of a magnetic-substance sheet and a dielectric sheet, contraction differed at the time of baking and it had the trouble of being hard to aim at improvement in dimensional accuracy.
[0005] This invention solves the above-mentioned trouble and it aims at offering the manufacture approach of solid-state composite part of having aimed at improvement in a property, and improvement in dimensional accuracy.
[0006]
[Means for Solving the Problem] In order to solve the above-mentioned trouble, while this invention forms an inductor conductor pattern layer on the whole surface of the 1st ceramic substrate The 1st process which forms a magnetic paste layer on said inductor conductor pattern layer, and forms the 1st substrate with an inductor layer, The capacitor conductor pattern layer which intervened the dielectric layer on the whole surface of the 2nd ceramic substrate is formed. While forming a glass paste layer at least in one side by the side of the 2nd process which forms the 2nd substrate with a capacitor layer, the whole surface of said 1st substrate, or the whole surface of said 2nd substrate The 3rd process which said the 1st substrate and said 2nd substrate are made to rival mutually through said glass paste layer, and forms tension coalesce, Calcinate said tension coalesce, and have the 4th process which forms a baking object, and the 5th process which forms an external electrode in said baking object, and the 1st non-calcinated ceramic substrate and the 2nd non-calcinated ceramic substrate are calcinated before said 1st process. It is the manufacture approach which established the process which forms the 1st ceramic substrate and 2nd ceramic substrate.

[0007] By the above-mentioned manufacture approach, since an inductor layer and a capacitor layer are formed on a ceramic substrate, improvement in a property can be aimed at.
[0008] Furthermore, since the 1st ceramic substrate and 2nd ceramic substrate calcinate and form the 1st non-calcinated ceramic substrate and the 2nd non-calcinated ceramic substrate which are a non-calcinated ceramic substrate, in case they calcinate tension coalesce and form a baking object, on the whole, the 1st ceramic substrate and 2nd ceramic substrate do not carry out the heat shrink of them. Thereby, while the inductor layer and capacitor layer which were formed on the 1st and 2nd ceramic substrate cannot contract and can raise dimensional accuracy to compensate for contraction of the 1st and 2nd ceramic substrate, in a back process etc., they do not need to adjust a dimension and can also simplify a production process.

[0009]
[Embodiment of the Invention] While invention of this invention according to claim 1 forms an inductor conductor pattern layer on the whole surface of the 1st ceramic substrate The 1st process which forms a magnetic paste layer on said inductor conductor pattern layer, and forms the 1st substrate with an inductor layer, The capacitor conductor pattern layer which intervened the dielectric layer on the whole surface of the 2nd ceramic substrate is formed. While forming a glass paste layer at least in one side by the side of the 2nd process which forms the 2nd substrate with a capacitor layer, the whole surface of said 1st substrate, or the whole surface of said 2nd substrate The 3rd process which said the 1st substrate and said 2nd substrate are made to rival mutually through said glass paste layer, and forms tension coalesce, Calcinate said tension coalesce, and have the 4th process which forms a baking object, and the 5th process which forms an external electrode in said baking object, and the 1st non-calcinated ceramic substrate and the 2nd non-calcinated ceramic substrate are calcinated before said 1st process. It is the manufacture approach which established the process which forms the 1st ceramic substrate and 2nd ceramic substrate.
[0010] By the above-mentioned manufacture approach, since an inductor layer and a capacitor layer are formed on a ceramic substrate, improvement in a property can be aimed at.
[0011] Furthermore, since the 1st ceramic substrate and 2nd ceramic substrate calcinate and form the 1st non-calcinated ceramic substrate and the 2nd non-calcinated ceramic substrate which are a non-calcinated ceramic substrate, in case they calcinate tension coalesce and form a baking object, on the whole, the 1st ceramic substrate and 2nd ceramic substrate do not carry out the heat shrink of them. Thereby, while the inductor layer and capacitor layer which were formed on the 1st and 2nd ceramic substrate cannot contract and can raise dimensional accuracy to compensate for contraction of the 1st and 2nd ceramic substrate, in a back process etc., they do not need to adjust a dimension and can also simplify a production process.
[0012] Invention of this invention according to claim 2 is set to invention according to claim 1. The 1st process The process which an inductor conductor pattern layer fills up with a conductive paste the pattern slot established in the front face of the intaglio which consists of a flexible resin substrate, and is dried, The process made to rival, heating and pressurizing said intaglio and whole surface of the 1st ceramic substrate, It is the manufacture approach which had and formed the process which exfoliates said intaglio from said 1st ceramic substrate, and imprints said conductive paste on said 1st ceramic substrate, and the process which calcinates said 1st ceramic substrate.
[0013] By the above-mentioned manufacture approach, the inductor conductor pattern layer with thick thickness with a sufficient pattern configuration which is FAIN wiring can be formed.
[0014] Invention of this invention according to claim 3 is the manufacture approach which established the process which forms the interlayer of a glass paste layer between the 2nd ceramic substrate and a capacitor layer in the 2nd process of invention according to claim 1.
[0015] By the above-mentioned manufacture approach, since the middle class of a glass paste layer is formed between the 2nd ceramic substrate and a capacitor layer, the effect from the 2nd substrate to a capacitor layer can be controlled.
[0016] Invention of this invention according to claim 4 is the manufacture approach which made the quality of the material of a glass paste layer the quality of the material with the glass frit which consists of any one of hoe silicic acid, a hoe lead silicate, a hoe calcium silicate, hoe aluminum silicate, and the hoe silicic acid titanium, its mixture, or its compound in invention according to claim 3.
[0017] By the above-mentioned manufacture approach, the effect from the 2nd ceramic substrate to a capacitor layer can be controlled.
[0018] In invention according to claim 1, in the 3rd process, invention of this invention according to claim 5 is the manufacture approach of solid-state composite part according to claim 1 of having established the process which carries out a debinder, after forming a glass paste layer.
[0019] By the above-mentioned manufacture approach, since the process which carries out a debinder is established after forming a glass paste layer, a void cannot occur but dependability can be raised.
[0020] In invention according to claim 1, while invention of this invention according to claim 6 forms two or more through tubes before the 4th process at the 2nd ceramic substrate It is the manufacture approach which established the process which forms a silver electrode in said through tube, established the process which forms baking ****** and established the process formed with said silver electrode at an external electrode in the 5th process after the 4th process so that a baking object might be divided into the piece of an individual and said silver electrode might express on a side face.
[0021] By the above-mentioned manufacture approach, since the gas which occurs from the middle class of a glass paste layer at the time of baking of tension coalesce since a through tube is formed in the 2nd ceramic substrate escapes from a through tube, a fine void cannot be generated, either but dependability can be raised very much.
[0022] Invention of this invention according to claim 7 is the manufacture approach which established the process which divides a baking object into the piece of an individual, and forms baking ****** after the 4th process in invention according to claim 1.

[0023] By the above-mentioned manufacture approach, mass production method can be made efficient. Invention of this invention according to claim 8 is the manufacture approach which established the process which carries out grinding of either [ at least ] the 1st ceramic substrate or the 2nd ceramic substrate, and makes thin one [ at least ] substrate thickness of the 1st ceramic substrate or the 2nd ceramic substrate after the 4th process in invention according to claim 1.
[0024] Thin shape-ization can be attained by the above-mentioned manufacture approach. Invention of this invention according to claim 9 is the manufacture approach by which the 1st ceramic substrate and 2nd ceramic substrate made the coefficient of thermal expansion equivalent mutually in invention according to claim 1.
[0025] By the above-mentioned manufacture approach, since the coefficient of thermal expansion of the 1st ceramic substrate and the 2nd ceramic substrate is mutually made equivalent and the expansion coefficient of the 1st and 2nd ceramic substrate at the time of baking of tension coalesce becomes equal, distortion etc. cannot arise but dimensional accuracy can be raised.
[0026] Invention of this invention according to claim 10 is the manufacture approach which made the quality of the material of the 1st ceramic substrate the quality of the material with a ferrite, and made the quality of the material of the 2nd ceramic substrate the quality of the material with forsterite in invention according to claim 9.
[0027] The good engine performance can be obtained by the above-mentioned manufacture approach. Invention of this invention according to claim 11 is the manufacture approach which made area of a capacitor conductor pattern layer larger than the area of a dielectric layer in invention according to claim 1.
[0028] By the above-mentioned manufacture approach, the effect from the interlayer of the 2nd ceramic substrate to a capacitor layer and a glass paste layer can be controlled.
[0029] Invention of this invention according to claim 12 is the manufacture approach which made the quality of the material of a capacitor conductor pattern layer the quality of the material with the glass frit which consists of any one of hoe silicic acid, a hoe lead silicate, a hoe calcium silicate, hoe aluminum silicate, and the hoe silicic acid titanium, its mixture, or its compound in invention according to claim 1.
[0030] By the above-mentioned manufacture approach, the effect of the dielectric on a capacitor conductor pattern layer can be controlled.
[0031] Invention of this invention according to claim 13 is the manufacture approach with the process which forms a two or more layers inductor conductor pattern layer in invention according to claim 1.
[0032] A good inductor layer can be formed by the above-mentioned manufacture approach. invention of this invention according to claim 14 -- invention according to claim 1 -- setting -- an inductor conductor pattern layer -- a line -- the conductor was made spiral -- spiral -- a conductor -- the section -- having -- said -- spiral -- a conductor -- said line of the section -- a conductor is the manufacture approach which exceeded 0.3 for the conductor thickness ratio to a conductor width.
[0033] spiral by the above-mentioned manufacture approach -- a conductor -- since the thickness of the section becomes thick, the inductor engine performance can be made good.
[0034] invention of this invention according to claim 15 -- invention according to claim 1 -- setting -- an inductor conductor pattern layer -- a line -- the conductor was made spiral -- spiral -- a conductor -- it has at least two sections and adjoins -- said -- spiral -- a conductor -- it is the manufacture approach which established the process which forms a non-magnetic material on ******.
[0035] The inductor engine performance can be made into high performance by the above-mentioned manufacture approach. invention of this invention according to claim 16 -- invention according to claim 1 -- setting -- an inductor conductor pattern layer -- a line -- the conductor was made spiral -- spiral -- a conductor -- it has at least two sections and adjoins -- said -- spiral -- a conductor -- while forming a non-magnetic material on ****** -- said -- spiral -- a conductor -- it is the manufacture approach which established the process which forms a slot in the 1st ceramic substrate on ******, and forms said non-magnetic material also in said slot.
[0036] The inductor engine performance can be made into high performance by the above-mentioned manufacture approach. invention of this invention according to claim 17 -- invention according to claim 1 -- setting -- an inductor conductor pattern layer -- a line -- the conductor was made spiral -- spiral -- a conductor -- the section and a line -- the shape of a ring which made the conductor the shape of a ring -- a conductor -- the section -- having -- said -- spiral -- a conductor -- the outside of the section -- the shape of said ring -- a conductor -- it is the manufacture approach which established the process which forms the section.
[0037] spiral by the above-mentioned manufacture approach -- a conductor -- an opposing magnetic field carries out a generating operation at the inductance by the section, frequency characteristics are prolonged, and the magnitude of attenuation good also in a RF field can be obtained.
[0038] invention of this invention according to claim 18 -- invention according to claim 1 -- setting -- an inductor conductor pattern layer -- a line -- the conductor was made spiral -- spiral -- a conductor -- the section and a line -- the shape of a ring which made the conductor the shape of a ring -- a conductor -- the section -- having -- said -- spiral -- a conductor -- the outside of the section -- the shape of said ring -- a conductor -- while forming the section -- the shape

of said ring -- a conductor -- it is the manufacture approach which established the process which forms the section into a magnetic paste layer.
[0039] the above-mentioned manufacture approach -- the shape of a ring -- a conductor -- much more spiral, since the section is formed into a magnetic paste layer -- a conductor -- an opposing magnetic field carries out a generating operation at the inductance by the section, frequency characteristics are prolonged, and the magnitude of attenuation good also in a RF field can be obtained.
[0040] invention of this invention according to claim 19 -- invention according to claim 17 -- setting -- the shape of a ring -- a conductor -- it is the manufacture approach which established the process which carries out ground connection of the section.
[0041] By the above-mentioned manufacture approach, the good magnitude of attenuation can be obtained in a RF field. invention of this invention according to claim 20 is spiral in invention according to claim 17 -- a conductor -- the shape of the section and a ring -- a conductor -- it is the manufacture approach which established the process which forms the section on the same flat surface at coincidence.
[0042] A production process can be simplified by the above-mentioned manufacture approach.
(Gestalt 1 of operation) Below, the manufacture approach of the solid-state composite part in the gestalt of 1 operation of this invention is explained, referring to a drawing.
[0043] In drawing 1 , when structural drawing of solid-state composite part is shown, the sectional view of the 1st ceramic substrate is shown in (a). The inductor electrode top view which is a spiral conductor pattern when making it the piece of an individual is shown in (b). The sectional view of the 2nd ceramic substrate is shown in (c). The sectional view at the time of making the 1st and 2nd ceramic substrate rival is shown in (d). The divided ceramic substrate sectional view is shown in (e).
[0044] The 1st non-calcinated ceramic substrate and the 2nd non-calcinated ceramic substrate are calcinated, and the 1st ceramic substrate 1 and 2nd ceramic substrate 4 are formed. On this 1st ceramic substrate 1, as an inductor conductor pattern layer, the inductor electrode 2 is formed, the ferrite layer 3 is formed as a magnetic paste layer on it, and an inductor layer is prepared. On the 2nd ceramic substrate 4, as a capacitor conductor pattern layer Prepare the capacitor layer which consists of the capacitor lower electrode 5, a capacitor up electrode 7, and a dielectric layer 6, and the adhesion glass layer 8 is applied at least to one side of the 1st and 2nd ceramic substrate 1 and 4 as a glass paste layer. Lamination and tension coalesce are formed mutually, this tension coalesce is calcinated, a baking object is formed, and the external electrode is formed in this baking object.
[0045] moreover, the inductor electrode 2 -- a line -- the conductor was made spiral -- spiral -- a conductor -- it forms by the section.
[0046] The manufacture approach is explained below. On the ceramic substrate 1, the pattern of the inductor electrode 2 was formed by the intaglio imprint using the silver paste, the substrate which performed pattern formation was calcinated by the peak temperature of 850 degrees C, and 10-minute maintenance, and the inductor electrode 2 was formed. At this time, the ratio of the thickness to the line breadth of the inductor electrode 2 was set to 0.4. On said inductor electrode 2, the ferrite paste performed the pattern of the ferrite layer 3, and it formed by screen-stencil, and the substrate which performed pattern formation was calcinated in 930 degrees C and 2 hours, and the ferrite layer 3 was formed. Next, the pattern of the capacitor lower electrode 5 is formed by screen-stencil with Ag paste which added the glass frit which consists of a hoe lead silicate on the 2nd ceramic substrate 4 with the almost same coefficient of thermal expansion as the 1st ceramic substrate 1, the pattern of a dielectric layer 6 is screen-stenciled on the capacitor lower electrode 5 using a dielectric paste, and the pattern of the capacitor up electrode 7 is formed by screen-stencil with Ag paste used for the lower electrode on a dielectric layer 6. This substrate is calcinated by the peak temperature of 900 degrees C, and 10-minute keeping, and a capacitor is formed. At this time, the pattern of the capacitor lower electrode 5 and the capacitor up electrode 7 was formed by the pattern which does not become smaller than a dielectric layer 6, and thickness could be 15 micrometers. Next, the pattern of the adhesion glass layer 8 was formed in the field which the inductor electrode 2 on said 1st ceramic substrate 1 formed by screen-stencil with a glass paste, and the debinder was performed in 500 degrees C and 30 minutes. And the adhesion glass layer 8 is pinched, lamination is performed for the 1st ceramic substrate 1 and the 2nd ceramic substrate 4, a substrate is calcinated by the peak temperature of 600 degrees C, and 10-minute maintenance, and the 1st ceramic substrate 1 and the 2nd ceramic substrate 4 are pasted up. In addition, the 2nd ceramic substrate 4 has turned the capacitor forming face to the glass layer side. After baking is completed, a substrate is cut to the piece of an individual and it becomes solid-state composite part by forming an external electrode (not shown) in a side face, a property is good by using the 1st and 2nd ceramic substrate 1 and 4, and since these ceramic substrates 1 and 4 have doubled the coefficient of thermal expansion, moreover, dimensional accuracy becomes good what has a short production process. Moreover, the engine performance of an inductor can be performed with a good thing because the ratio of the thickness to the line breadth of the inductor electrode 2 thickened thickness exceeding 0.3. moreover, the capacitor which puts the dielectric layer 6 of the 2nd ceramic substrate 4 -- the effect of a substrate, a glass layer, and the dielectric layer 6 on the electrode itself can be controlled by having added the glass frit which sets a conductor to 10 micrometers or more

at least, forms the thickness after baking in the size which does not become smaller than the pattern size of a dielectric layer 6, and consists of a HOU lead silicate. Moreover, in order to carry out the debinder of the adhesion glass layer 8 for pasting up said the 1st ceramic substrate 1 and said 2nd ceramic substrate 4 before adhesion, a void is hard to generate it. The reliable manufacture approach of solid-state composite part can be offered from the above thing.

[0047] (Gestalt 2 of operation) Below, the manufacture approach of the solid-state composite part of an example of the manufacture approach of the electronic parts of this invention is explained, referring to a drawing.

[0048] When structural drawing of solid-state composite part is shown in drawing 2 , the sectional view of a ferrite substrate is shown in (a). The inductor electrode top view which is a spiral conductor pattern when making it the piece of an individual is shown in (b). The ring-like electrode top view on the ferrite layer when making it the piece of an individual is shown in (c). The sectional view of a forsterite substrate is shown in (d). The sectional view at the time of making a ferrite substrate and a forsterite substrate rival is shown in (e). The divided substrate sectional view is shown in (f). The inductor electrode 12 is first formed on the ferrite substrate 11, the ferrite layer 13 is formed on it, and the ring-like electrode 14 is formed on it. The capacitor which consists of the glass layer 16, the capacitor lower electrode 17, a dielectric layer 18, and a capacitor up electrode 19 is formed on the forsterite substrate 15, it pastes up on both sides of the adhesion glass layer 20, and the ferrite substrate 11 and the forsterite substrate 15 are cut to the piece of an individual after that.

[0049] The manufacture approach is explained below. On the ferrite substrate 11, the pattern of the inductor electrode 12 was formed by the intaglio imprint using the paste of silver and palladium, the substrate which performed pattern formation was calcinated by the peak temperature of 850 degrees C, and 10-minute maintenance, and the inductor electrode 12 was formed. At this time, the ratio of the thickness to the line breadth of the inductor electrode 12 was set to 0.8. Said inductor electrode 12 was formed upwards, a ferrite paste is used, the pattern of the ferrite layer 13 is formed by screen-stencil, it calcinates in 950 degrees C and 3 hours, and the ferrite layer 13 is formed. On said ferrite layer 13, the pattern of the ring-like electrode 14 was formed by screen-stencil using the paste of silver and palladium, the substrate which performed pattern formation was calcinated by the peak temperature of 850 degrees C, and 10-minute maintenance, and the ring-like electrode 14 was formed. Next, on the forsterite substrate 15 with the almost same coefficient of thermal expansion as said ferrite substrate 11, the pattern of the glass layer 16 is formed by screen-stencil using the glass paste which consists of hoe silicic acid titanium, it calcinates by the peak temperature of 900 degrees C, and 10-minute keeping, and the glass layer 16 is formed. And the pattern of the capacitor lower electrode 17 is formed by screen-stencil on the glass layer 16 with the silver and the palladium paste which added the glass frit which consists of hoe aluminum silicate, and the pattern of the capacitor up electrode 19 is formed by screen-stencil on the capacitor lower electrode 17 using a dielectric paste with the silver and the palladium paste which formed by screen-stencil and used the pattern of a dielectric layer 18 for the lower electrode on the dielectric layer 18. This substrate is calcinated by the peak temperature of 850 degrees C, and 10-minute keeping, and a capacitor is formed. At this time, the pattern of the capacitor lower electrode 17 and the capacitor up electrode 19 was formed by the pattern which does not become smaller than a dielectric layer 18, and thickness could be 20 micrometers. Next, the pattern of the adhesion glass layer 20 was formed in the field which the inductor electrode 12 on the ferrite substrate 11 formed, and the field in which the capacitor of the forsterite substrate 15 was formed, by screen-stencil with a glass paste, and the debinder was performed in 500 degrees C and 30 minutes. And on both sides of the adhesion glass layer 20, lamination is performed for the ferrite substrate 11 and the forsterite substrate 15, a substrate is calcinated by the peak temperature of 700 degrees C, and 10-minute maintenance, and the ferrite substrate 11 and the forsterite substrate 15 are pasted up. After baking is completed, a substrate is cut to the piece of an individual and it becomes solid-state composite part by forming an external electrode (******) in a side face, and since substrates 11 and 15 have doubled the coefficient of thermal expansion, dimensional accuracy will become good. Moreover, even if it forms two or more inductor electrodes 14 into one component, the engine performance of an inductor can be made good, because the ratio of the thickness to the line breadth of the inductor electrode 12 thickened thickness exceeding 0.3, formed the non-magnetic material between patterns and formed the ring-like electrode 14 on the inductor electrode 12. moreover, the capacitor which forms the glass layer 16 which consists of hoe silicic acid titanium, and puts a dielectric layer 18 between the bottom of a capacitor -- the effect of a substrate, a glass layer, and the dielectric layer 18 on the electrode itself can be controlled by having added the glass frit which sets thickness to 10 micrometers or more, forms it in the size which does not become smaller than the pattern size of a dielectric layer 18, and consists a conductor of HOU aluminum silicate in it. Moreover, in order to carry out the debinder of the glass layer 16 for pasting up said ferrite substrate 11 and said forsterite substrate 15 before adhesion, a void is hard to generate it. The reliable manufacture approach of solid-state composite part can be offered from the above thing.

[0050] (Gestalt 3 of operation) Below, the manufacture approach of the solid-state composite part of an example of the manufacture approach of the electronic parts of this invention is explained, referring to a drawing.

[0051] When structural drawing of solid-state composite part is shown in drawing 3 , the sectional view of a ferrite substrate is shown in (a). The inductor electrode top view which is a spiral conductor pattern when making it the piece

of an individual is shown in (b). The top view of the forsterite substrate in which the through tube was formed is shown in (c). The sectional view of a forsterite substrate is shown in (d). The sectional view at the time of making a ferrite substrate and a forsterite substrate rival is shown in (e). The divided substrate sectional view is shown in (f). First, the nonmagnetic glass layer 22 and the inductor electrode 23 are formed on the ferrite substrate 21, and the ferrite layer 24 is formed on these. After forming a through tube 26 in the forsterite substrate 25, the capacitor which consists of the capacitor lower electrode 27, a dielectric layer 28, and a capacitor up electrode 29 is formed on said forsterite substrate 25, it pastes up on both sides of the adhesion glass layer 30, and the ferrite substrate 21 and the forsterite substrate 25 are cut to the piece of an individual.

[0052] The manufacture approach is explained below. Formation is used on the ferrite substrate 21, a glass paste is used for this slot for a slot, the pattern of the nonmagnetic glass layer 22 is formed by screen-stencil, it calcinates in the peak temperature of 900 degrees C, and 10 minutes, and the glass layer 22 is formed. And by intaglio imprint, the pattern of the inductor electrode 23 was formed using the paste of silver and palladium, the substrate which performed pattern formation was calcinated by the peak temperature of 850 degrees C, and 10-minute maintenance, and the inductor electrode 23 was formed. At this time, the ratio of the thickness to the line breadth of the inductor electrode 23 was set to 1.5. Said inductor electrode 23 was formed upwards, a ferrite paste is used, the pattern of the ferrite layer 24 is formed by screen-stencil, it calcinates in 950 degrees C and 3 hours, and the ferrite layer 24 is formed. Next, on the forsterite substrate 25 with the almost same coefficient of thermal expansion as said ferrite substrate 21 in which the through tube 26 was formed The pattern of the capacitor lower electrode 27 is formed by screen-stencil with the silver and the platinum paste which added the glass frit which consists of a hoe calcium silicate. The pattern of a dielectric layer 28 is formed by screen-stencil on the capacitor lower electrode 27 using a dielectric paste, and the pattern of the capacitor up electrode 29 is formed by screen-stencil with the silver and the platinum paste used with the capacitor lower electrode 27 on the dielectric layer 28. This substrate is calcinated by the peak temperature of 900 degrees C, and 10-minute keeping, and a capacitor is formed. At this time, the pattern of the capacitor lower electrode 27 and the capacitor up electrode 29 was formed by the pattern which does not become smaller than a dielectric layer 28, and thickness could be 13 micrometers. Next, the pattern of the adhesion glass layer 30 was formed in the field in which the inductor electrode 23 on the ferrite substrate 21 was formed, and the field in which the capacitor of the forsterite substrate 25 was formed, by screen-stencil with a glass paste, and the debinder was performed in 500 degrees C and 30 minutes. And on both sides of the adhesion glass layer 30, lamination is performed for the ferrite substrate 21 and the forsterite substrate 25, a substrate is calcinated by the peak temperature of 680 degrees C, and 10-minute maintenance, and the ferrite substrate 1 and the forsterite substrate 25 are pasted up. After baking is completed, a substrate is cut to the piece of an individual and it becomes solid-state composite part by forming an external electrode (not shown) in a side face, and since the ferrite substrate 21 and the forsterite substrate 25 have doubled the coefficient of thermal expansion, dimensional accuracy will become good. Moreover, the ratio of the thickness to the line breadth of the inductor electrode 23 thickens thickness exceeding 0.3, and by having formed in the slot between patterns the glass layer which is a non-magnetic material, even if it forms two or more inductor electrodes 23 into one component, the engine performance of an inductor can be made good. moreover, the capacitor which puts a dielectric layer 28 -- the effect of a substrate, a glass layer, and the dielectric layer 28 on the electrode itself can be controlled by having added the glass frit which sets thickness to 10 micrometers or more, forms it in the size which does not become smaller than the pattern size of a dielectric layer 28, and consists a conductor of a HOU calcium silicate in it. Moreover, the adhesion glass layer 30 for pasting up said ferrite substrate 21 and said forsterite substrate 25 is having formed the through tube 26 in the forsterite substrate 25 beforehand, since the occurring gas falls out to a through tube 26 at the time of baking of a glue line, does not generate a fine void, either but can acquire higher dependability. The reliable manufacture approach of solid-state composite part can be offered from the above thing.

[0053] (Gestalt 4 of operation) Below, the manufacture approach of the solid-state composite part of an example of the manufacture approach of the electronic parts of this invention is explained, referring to a drawing.

[0054] When structural drawing of solid-state composite part is shown in drawing 4 , the sectional view of a ferrite substrate is shown in (a). The inductor electrode top view which is a spiral conductor pattern when making it the piece of an individual is shown in (b). The sectional view of a forsterite substrate is shown in (c). The sectional view at the time of making a ferrite substrate and a forsterite substrate rival is shown in (d). The divided substrate sectional view is shown in (e). First, the inductor electrode 32, the ring-like electrode 33, and the nonmagnetic glass layer 34 are formed on the ferrite substrate 31, and the ferrite layer 35 is formed on these. The glass layer 37 is formed on the forsterite substrate 36, the capacitor which consists of the capacitor lower electrode 38, a dielectric layer 39, and a capacitor up electrode 40 is formed on said glass layer 37, it pastes up on both sides of the adhesion glass layer 41, and the ferrite substrate 31 and the forsterite substrate 36 are cut to the piece of an individual.

[0055] The manufacture approach is explained below. The pattern of the inductor electrode 32 and the ring-like electrode 33 was formed by intaglio imprint on the ferrite substrate 31 using the silver paste, the substrate which performed pattern formation was calcinated by the peak temperature of 900 degrees C, and 10-minute maintenance,

and the inductor electrode 32 and the ring-like electrode 33 were formed. At this time, the ratio of the thickness to the line breadth of the inductor electrode 32 was set to 1.5. Moreover, said ring-like electrode 33 is connected by beer (not shown). On the substrate in which said electrode was formed, a glass paste is used, the pattern of the nonmagnetic glass layer 34 is formed by screen-stencil, it calcinates in the peak temperature of 900 degrees C, and 10 minutes, and the glass layer 34 is formed. Said inductor electrode 32 was formed upwards, a ferrite paste is used, the pattern of the ferrite layer 35 is formed by screen-stencil, it calcinates in 970 degrees C and 3 hours, and the ferrite layer 35 is formed. Next, on the forsterite substrate 36 with the almost same coefficient of thermal expansion as said ferrite substrate 31, the paste of boro-silicated glass is used, the pattern of the glass layer 37 is formed by screen-stencil, it calcinates by the peak temperature of 900 degrees C, and 10-minute keeping, and the glass layer 37 is formed. And the pattern of the capacitor lower electrode 38 is formed by screen-stencil on the glass layer 37 with the silver and the platinum paste which added the glass frit which consists of hoe silicic acid titanium, the pattern of a dielectric layer 39 is formed by screen-stencil on the capacitor lower electrode 38 using a dielectric paste, and the pattern of the capacitor up electrode 40 is formed by screen-stencil with the silver and the platinum paste used with the capacitor lower electrode 38 on the dielectric layer 39. This substrate is calcinated by the peak temperature of 900 degrees C, and 10-minute keeping, and a capacitor is formed. At this time, the pattern of the capacitor lower electrode 38 and the capacitor up electrode 40 was formed by the pattern which does not become smaller than a dielectric layer 39, and thickness could be 13 micrometers. Next, the pattern of the adhesion glass layer 41 was formed in the field in which the inductor electrode 32 on the ferrite substrate 31 was formed, and the field in which the capacitor of the forsterite substrate 36 was formed, by screen-stencil with a glass paste, and the debinder was performed in 500 degrees C and 30 minutes. And on both sides of the adhesion glass layer 41, lamination is performed for the ferrite substrate 31 and the forsterite substrate 36, a substrate is calcinated by the peak temperature of 730 degrees C, and 10-minute maintenance, and the ferrite substrate 31 and the forsterite substrate 36 are pasted up. After baking is completed, a substrate is cut to the piece of an individual and it becomes solid-state composite part by forming an external electrode (not shown) in a side face.

[0056] In addition, since substrates 31 and 36 have doubled the coefficient of thermal expansion, dimensional accuracy will become good. Moreover, by the ratio of the thickness to the line breadth of the inductor electrode 32 having thickened thickness exceeding 0.3, having formed the glass layer which is a non-magnetic material between patterns, and having formed the ring-like electrode 33 around inductor electrode 32, even if it forms two or more inductor electrodes 32 into one component, the engine performance of an inductor can be made good. moreover, the capacitor which forms the boro-silicated glass layer 37 in the bottom of a capacitor, and puts a dielectric layer 39 -- the effect of a substrate, a glass layer, and the dielectric layer 39 on the electrode itself can be controlled by having added the glass frit which sets thickness to 10 micrometers or more, forms it in the size which does not become smaller than the pattern size of a dielectric layer 39, and consists a conductor of hoe silicic acid titanium in it. The reliable manufacture approach of solid-state composite part can be offered from the above thing.

[0057] In addition, although the example of the gestalt of four operations explained in the above explanation, in a wiring substrate which needs electrode wiring which makes a coefficient of thermal expansion almost the same, it can carry out similarly. Furthermore, although a spiral conductor pattern is the thing of a monolayer and is performed with the above-mentioned operation gestalt, even if it forms in two or more layers, the same solid-state composite part is obtained. Moreover, a spiral conductor pattern can be similarly carried out, if it is the wiring electrode pattern of a configuration of that it can be used as an inductor electrode.

[0058] Moreover, even if it carries out grinding at least of one side and makes substrate thickness thin after joining the 1st and 2nd ceramic substrate by the glue line, the same solid-state composite part is obtained. a capacitor -- although it is four kinds of things and being explained to the glass frit used for a conductor, if it becomes, it will be the thing which is the glass frit which consists of hoe silicic acid, a hoe lead silicate, a hoe calcium silicate, hoe aluminum silicate, hoe silicic acid titanium, mixture, or a compound and from which the same effectiveness is acquired. Moreover, although the glass layers formed in the bottom of a capacitor are two kinds of things and are explained, the same effectiveness will be acquired if it is the glass frit which consists of hoe silicic acid, a hoe lead silicate, a hoe calcium silicate, hoe aluminum silicate, hoe silicic acid titanium, mixture, or a compound.

[0059]

[Effect of the Invention] Since an inductor layer and a capacitor layer are formed on a ceramic substrate as mentioned above according to this invention, improvement in a property can be aimed at.

[0060] Furthermore, since the 1st ceramic substrate and 2nd ceramic substrate calcinate and form the 1st non-calcinated ceramic substrate and the 2nd non-calcinated ceramic substrate which are a non-calcinated ceramic substrate, in case they calcinate tension coalesce and form a baking object, on the whole, the 1st ceramic substrate and 2nd ceramic substrate do not carry out the heat shrink of them. Thereby, while the inductor layer and capacitor layer which were formed on the 1st and 2nd ceramic substrate cannot contract and can raise dimensional accuracy to compensate for contraction of the 1st and 2nd ceramic substrate, in a back process etc., they do not need to adjust a dimension and can also simplify a production process.

[0061] Consequently, the manufacture approach of solid-state composite part of having aimed at improvement in a property and improvement in dimensional accuracy can be offered.

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[Translation done.]

## TECHNICAL FIELD

[Field of the Invention] This invention relates to the manufacture approach of the solid-state composite part of the chip mold which the inductor, the capacitor, etc. compounded.

[Translation done.]

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PRIOR ART

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[Description of the Prior Art] In recent years, small and lightweight-ization are progressing, Semi-conductor LSI, a chip, etc. have the demand of a miniaturization also with a high frequency-related magnetic device in this, the demand of a miniaturization of the capacitor which used the dielectric of a thick film increases, and the approach of making a dielectric and an inductor unification and making them small into one device, etc. has been developed.
[0003] the capacitor formation approach of having attained the miniaturization -- JP,2-54647,B -- setting -- a nonmagnetic insulator layer and the electrode for capacitors -- a conductor -- crosswise lamination -- carrying out -- the nonmagnetic insulator layer of the still more nearly same quality of the material on it, and the object for coils -- crosswise lamination of the conductor is carried out and the method of really calcinating these, compound-izing an inductor and a capacitor, and attaining a miniaturization is introduced. Moreover, as the manufacture approach of simpler solid-state composite part, a magnetic-substance sheet and a dielectric sheet are calcinated and the method of carrying out lamination unification by the interlayer is introduced as indicated by JP,57-193019,A.

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[Translation done.]

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## EFFECT OF THE INVENTION

[Effect of the Invention] Since an inductor layer and a capacitor layer are formed on a ceramic substrate as mentioned above according to this invention, improvement in a property can be aimed at.
[0060] Furthermore, since the 1st ceramic substrate and 2nd ceramic substrate calcinate and form the 1st non-calcinated ceramic substrate and the 2nd non-calcinated ceramic substrate which are a non-calcinated ceramic substrate, in case they calcinate tension coalesce and form a baking object, on the whole, the 1st ceramic substrate and 2nd ceramic substrate do not carry out the heat shrink of them. Thereby, while the inductor layer and capacitor layer which were formed on the 1st and 2nd ceramic substrate cannot contract and can raise dimensional accuracy to compensate for contraction of the 1st and 2nd ceramic substrate, in a back process etc., they do not need to adjust a dimension and can also simplify a production process.
[0061] Consequently, the manufacture approach of solid-state composite part of having aimed at improvement in a property and improvement in dimensional accuracy can be offered.

[Translation done.]

## TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] By the above-mentioned conventional approach, in order to really calcinate an inductor and a capacitor, a magnetic-substance sheet and a dielectric sheet need to use low-temperature-sintering material, and it is hard to aim at improvement in a property. Moreover, from the difference in the coefficient of thermal expansion of a magnetic-substance sheet and a dielectric sheet, contraction differed at the time of baking and it had the trouble of being hard to aim at improvement in dimensional accuracy.
[0005] This invention solves the above-mentioned trouble and it aims at offering the manufacture approach of solid-state composite part of having aimed at improvement in a property, and improvement in dimensional accuracy.

[Translation done.]

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MEANS

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[Means for Solving the Problem] In order to solve the above-mentioned trouble, while this invention forms an inductor conductor pattern layer on the whole surface of the 1st ceramic substrate The 1st process which forms a magnetic paste layer on said inductor conductor pattern layer, and forms the 1st substrate with an inductor layer, The capacitor conductor pattern layer which intervened the dielectric layer on the whole surface of the 2nd ceramic substrate is formed. While forming a glass paste layer at least in one side by the side of the 2nd process which forms the 2nd substrate with a capacitor layer, the whole surface of said 1st substrate, or the whole surface of said 2nd substrate The 3rd process which said the 1st substrate and said 2nd substrate are made to rival mutually through said glass paste layer, and forms tension coalesce, Calcinate said tension coalesce, and have the 4th process which forms a baking object, and the 5th process which forms an external electrode in said baking object, and the 1st non-calcinated ceramic substrate and the 2nd non-calcinated ceramic substrate are calcinated before said 1st process. It is the manufacture approach which established the process which forms the 1st ceramic substrate and 2nd ceramic substrate.

[0007] By the above-mentioned manufacture approach, since an inductor layer and a capacitor layer are formed on a ceramic substrate, improvement in a property can be aimed at.
[0008] Furthermore, since the 1st ceramic substrate and 2nd ceramic substrate calcinate and form the 1st non-calcinated ceramic substrate and the 2nd non-calcinated ceramic substrate which are a non-calcinated ceramic substrate, in case they calcinate tension coalesce and form a baking object, on the whole, the 1st ceramic substrate and 2nd ceramic substrate do not carry out the heat shrink of them. Thereby, while the inductor layer and capacitor layer which were formed on the 1st and 2nd ceramic substrate cannot contract and can raise dimensional accuracy to compensate for contraction of the 1st and 2nd ceramic substrate, in a back process etc., they do not need to adjust a dimension and can also simplify a production process.
[0009]
[Embodiment of the Invention] While invention of this invention according to claim 1 forms an inductor conductor pattern layer on the whole surface of the 1st ceramic substrate The 1st process which forms a magnetic paste layer on said inductor conductor pattern layer, and forms the 1st substrate with an inductor layer, The capacitor conductor pattern layer which intervened the dielectric layer on the whole surface of the 2nd ceramic substrate is formed. While forming a glass paste layer at least in one side by the side of the 2nd process which forms the 2nd substrate with a capacitor layer, the whole surface of said 1st substrate, or the whole surface of said 2nd substrate The 3rd process which said the 1st substrate and said 2nd substrate are made to rival mutually through said glass paste layer, and forms tension coalesce, Calcinate said tension coalesce, and have the 4th process which forms a baking object, and the 5th process which forms an external electrode in said baking object, and the 1st non-calcinated ceramic substrate and the 2nd non-calcinated ceramic substrate are calcinated before said 1st process. It is the manufacture approach which established the process which forms the 1st ceramic substrate and 2nd ceramic substrate.
[0010] By the above-mentioned manufacture approach, since an inductor layer and a capacitor layer are formed on a ceramic substrate, improvement in a property can be aimed at.
[0011] Furthermore, since the 1st ceramic substrate and 2nd ceramic substrate calcinate and form the 1st non-calcinated ceramic substrate and the 2nd non-calcinated ceramic substrate which are a non-calcinated ceramic substrate, in case they calcinate tension coalesce and form a baking object, on the whole, the 1st ceramic substrate and 2nd ceramic substrate do not carry out the heat shrink of them. Thereby, while the inductor layer and capacitor layer which were formed on the 1st and 2nd ceramic substrate cannot contract and can raise dimensional accuracy to compensate for contraction of the 1st and 2nd ceramic substrate, in a back process etc., they do not need to adjust a dimension and can also simplify a production process.
[0012] Invention of this invention according to claim 2 is set to invention according to claim 1. The 1st process The process which an inductor conductor pattern layer fills up with a conductive paste the pattern slot established in the front face of the intaglio which consists of a flexible resin substrate, and is dried, The process made to rival, heating and pressurizing said intaglio and whole surface of the 1st ceramic substrate, It is the manufacture approach which

had and formed the process which exfoliates said intaglio from said 1st ceramic substrate, and imprints said conductive paste on said 1st ceramic substrate, and the process which calcinates said 1st ceramic substrate.
[0013] By the above-mentioned manufacture approach, the inductor conductor pattern layer with thick thickness with a sufficient pattern configuration which is FAIN wiring can be formed.
[0014] Invention of this invention according to claim 3 is the manufacture approach which established the process which forms the interlayer of a glass paste layer between the 2nd ceramic substrate and a capacitor layer in the 2nd process of invention according to claim 1.
[0015] By the above-mentioned manufacture approach, since the middle class of a glass paste layer is formed between the 2nd ceramic substrate and a capacitor layer, the effect from the 2nd substrate to a capacitor layer can be controlled.
[0016] Invention of this invention according to claim 4 is the manufacture approach which made the quality of the material of a glass paste layer the quality of the material with the glass frit which consists of any one of hoe silicic acid, a hoe lead silicate, a hoe calcium silicate, hoe aluminum silicate, and the hoe silicic acid titanium, its mixture, or its compound in invention according to claim 3.
[0017] By the above-mentioned manufacture approach, the effect from the 2nd ceramic substrate to a capacitor layer can be controlled.
[0018] In invention according to claim 1, in the 3rd process, invention of this invention according to claim 5 is the manufacture approach of solid-state composite part according to claim 1 of having established the process which carries out a debinder, after forming a glass paste layer.
[0019] By the above-mentioned manufacture approach, since the process which carries out a debinder is established after forming a glass paste layer, a void cannot occur but dependability can be raised.
[0020] In invention according to claim 1, while invention of this invention according to claim 6 forms two or more through tubes before the 4th process at the 2nd ceramic substrate It is the manufacture approach which established the process which forms a silver electrode in said through tube, established the process which forms baking ****** and established the process formed with said silver electrode at an external electrode in the 5th process after the 4th process so that a baking object might be divided into the piece of an individual and said silver electrode might express on a side face.
[0021] By the above-mentioned manufacture approach, since the gas which occurs from the middle class of a glass paste layer at the time of baking of tension coalesce since a through tube is formed in the 2nd ceramic substrate escapes from a through tube, a fine void cannot be generated, either but dependability can be raised very much.
[0022] Invention of this invention according to claim 7 is the manufacture approach which established the process which divides a baking object into the piece of an individual, and forms baking ****** after the 4th process in invention according to claim 1.
[0023] By the above-mentioned manufacture approach, mass production method can be made efficient. Invention of this invention according to claim 8 is the manufacture approach which established the process which carries out grinding of either [ at least ] the 1st ceramic substrate or the 2nd ceramic substrate, and makes thin one [ at least ] substrate thickness of the 1st ceramic substrate or the 2nd ceramic substrate after the 4th process in invention according to claim 1.
[0024] Thin shape-ization can be attained by the above-mentioned manufacture approach. Invention of this invention according to claim 9 is the manufacture approach by which the 1st ceramic substrate and 2nd ceramic substrate made the coefficient of thermal expansion equivalent mutually in invention according to claim 1.
[0025] By the above-mentioned manufacture approach, since the coefficient of thermal expansion of the 1st ceramic substrate and the 2nd ceramic substrate is mutually made equivalent and the expansion coefficient of the 1st and 2nd ceramic substrate at the time of baking of tension coalesce becomes equal, distortion etc. cannot arise but dimensional accuracy can be raised.
[0026] Invention of this invention according to claim 10 is the manufacture approach which made the quality of the material of the 1st ceramic substrate the quality of the material with a ferrite, and made the quality of the material of the 2nd ceramic substrate the quality of the material with forsterite in invention according to claim 9.
[0027] The good engine performance can be obtained by the above-mentioned manufacture approach. Invention of this invention according to claim 11 is the manufacture approach which made area of a capacitor conductor pattern layer larger than the area of a dielectric layer in invention according to claim 1.
[0028] By the above-mentioned manufacture approach, the effect from the interlayer of the 2nd ceramic substrate to a capacitor layer and a glass paste layer can be controlled.
[0029] Invention of this invention according to claim 12 is the manufacture approach which made the quality of the material of a capacitor conductor pattern layer the quality of the material with the glass frit which consists of any one of hoe silicic acid, a hoe lead silicate, a hoe calcium silicate, hoe aluminum silicate, and the hoe silicic acid titanium, its mixture, or its compound in invention according to claim 1.
[0030] By the above-mentioned manufacture approach, the effect of the dielectric on a capacitor conductor pattern

layer can be controlled.
[0031] Invention of this invention according to claim 13 is the manufacture approach with the process which forms a two or more layers inductor conductor pattern layer in invention according to claim 1.
[0032] A good inductor layer can be formed by the above-mentioned manufacture approach. invention of this invention according to claim 14 -- invention according to claim 1 -- setting -- an inductor conductor pattern layer -- a line -- the conductor was made spiral -- spiral -- a conductor -- the section -- having -- said -- spiral -- a conductor -- said line of the section -- a conductor is the manufacture approach which exceeded 0.3 for the conductor thickness ratio to a conductor width.
[0033] spiral by the above-mentioned manufacture approach -- a conductor -- since the thickness of the section becomes thick, the inductor engine performance can be made good.
[0034] invention of this invention according to claim 15 -- invention according to claim 1 -- setting -- an inductor conductor pattern layer -- a line -- the conductor was made spiral -- spiral -- a conductor -- it has at least two sections and adjoins -- said -- spiral -- a conductor -- it is the manufacture approach which established the process which forms a non-magnetic material on ******.
[0035] The inductor engine performance can be made into high performance by the above-mentioned manufacture approach. invention of this invention according to claim 16 -- invention according to claim 1 -- setting -- an inductor conductor pattern layer -- a line -- the conductor was made spiral -- spiral -- a conductor -- it has at least two sections and adjoins -- said -- spiral -- a conductor -- while forming a non-magnetic material on ****** -- said -- spiral -- a conductor -- it is the manufacture approach which established the process which forms a slot in the 1st ceramic substrate on ******, and forms said non-magnetic material also in said slot.
[0036] The inductor engine performance can be made into high performance by the above-mentioned manufacture approach. invention of this invention according to claim 17 -- invention according to claim 1 -- setting -- an inductor conductor pattern layer -- a line -- the conductor was made spiral -- spiral -- a conductor -- the section and a line -- the shape of a ring which made the conductor the shape of a ring -- a conductor -- the section -- having -- said -- spiral -- a conductor -- the outside of the section -- the shape of said ring -- a conductor -- it is the manufacture approach which established the process which forms the section.
[0037] spiral by the above-mentioned manufacture approach -- a conductor -- an opposing magnetic field carries out a generating operation at the inductance by the section, frequency characteristics are prolonged, and the magnitude of attenuation good also in a RF field can be obtained.
[0038] invention of this invention according to claim 18 -- invention according to claim 1 -- setting -- an inductor conductor pattern layer -- a line -- the conductor was made spiral -- spiral -- a conductor -- the section and a line -- the shape of a ring which made the conductor the shape of a ring -- a conductor -- the section -- having -- said -- spiral -- a conductor -- the outside of the section -- the shape of said ring -- a conductor -- while forming the section -- the shape of said ring -- a conductor -- it is the manufacture approach which established the process which forms the section into a magnetic paste layer.
[0039] the above-mentioned manufacture approach -- the shape of a ring -- a conductor -- much more spiral, since the section is formed into a magnetic paste layer -- a conductor -- an opposing magnetic field carries out a generating operation at the inductance by the section, frequency characteristics are prolonged, and the magnitude of attenuation good also in a RF field can be obtained.
[0040] invention of this invention according to claim 19 -- invention according to claim 17 -- setting -- the shape of a ring -- a conductor -- it is the manufacture approach which established the process which carries out ground connection of the section.
[0041] By the above-mentioned manufacture approach, the good magnitude of attenuation can be obtained in a RF field. invention of this invention according to claim 20 is spiral in invention according to claim 17 -- a conductor -- the shape of the section and a ring -- a conductor -- it is the manufacture approach which established the process which forms the section on the same flat surface at coincidence.
[0042] A production process can be simplified by the above-mentioned manufacture approach.
(Gestalt 1 of operation) Below, the manufacture approach of the solid-state composite part in the gestalt of 1 operation of this invention is explained, referring to a drawing.
[0043] In drawing 1 , when structural drawing of solid-state composite part is shown, the sectional view of the 1st ceramic substrate is shown in (a). The inductor electrode top view which is a spiral conductor pattern when making it the piece of an individual is shown in (b). The sectional view of the 2nd ceramic substrate is shown in (c). The sectional view at the time of making the 1st and 2nd ceramic substrate rival is shown in (d). The divided ceramic substrate sectional view is shown in (e).
[0044] The 1st non-calcinated ceramic substrate and the 2nd non-calcinated ceramic substrate are calcinated, and the 1st ceramic substrate 1 and 2nd ceramic substrate 4 are formed. On this 1st ceramic substrate 1, as an inductor conductor pattern layer, the inductor electrode 2 is formed, the ferrite layer 3 is formed as a magnetic paste layer on it, and an inductor layer is prepared. On the 2nd ceramic substrate 4, as a capacitor conductor pattern layer Prepare the

çapacitor layer which consists of the capacitor lower electrode 5, a capacitor up electrode 7, and a dielectric layer 6, and the adhesion glass layer 8 is applied at least to one side of the 1st and 2nd ceramic substrate 1 and 4 as a glass paste layer. Lamination and tension coalesce are formed mutually, this tension coalesce is calcinated, a baking object is formed, and the external electrode is formed in this baking object.
[0045] moreover, the inductor electrode 2 -- a line -- the conductor was made spiral -- spiral -- a conductor -- it forms by the section.
[0046] The manufacture approach is explained below. On the ceramic substrate 1, the pattern of the inductor electrode 2 was formed by the intaglio imprint using the silver paste, the substrate which performed pattern formation was calcinated by the peak temperature of 850 degrees C, and 10-minute maintenance, and the inductor electrode 2 was formed. At this time, the ratio of the thickness to the line breadth of the inductor electrode 2 was set to 0.4. On said inductor electrode 2, the ferrite paste performed the pattern of the ferrite layer 3, and it formed by screen-stencil, and the substrate which performed pattern formation was calcinated in 930 degrees C and 2 hours, and the ferrite layer 3 was formed. Next, the pattern of the capacitor lower electrode 5 is formed by screen-stencil with Ag paste which added the glass frit which consists of a hoe lead silicate on the 2nd ceramic substrate 4 with the almost same coefficient of thermal expansion as the 1st ceramic substrate 1, the pattern of a dielectric layer 6 is screen-stenciled on the capacitor lower electrode 5 using a dielectric paste, and the pattern of the capacitor up electrode 7 is formed by screen-stencil with Ag paste used for the lower electrode on a dielectric layer 6. This substrate is calcinated by the peak temperature of 900 degrees C, and 10-minute keeping, and a capacitor is formed. At this time, the pattern of the capacitor lower electrode 5 and the capacitor up electrode 7 was formed by the pattern which does not become smaller than a dielectric layer 6, and thickness could be 15 micrometers. Next, the pattern of the adhesion glass layer 8 was formed in the field which the inductor electrode 2 on said 1st ceramic substrate 1 formed by screen-stencil with a glass paste, and the debinder was performed in 500 degrees C and 30 minutes. And the adhesion glass layer 8 is pinched, lamination is performed for the 1st ceramic substrate 1 and the 2nd ceramic substrate 4, a substrate is calcinated by the peak temperature of 600 degrees C, and 10-minute maintenance, and the 1st ceramic substrate 1 and the 2nd ceramic substrate 4 are pasted up. In addition, the 2nd ceramic substrate 4 has turned the capacitor forming face to the glass layer side. After baking is completed, a substrate is cut to the piece of an individual and it becomes solid-state composite part by forming an external electrode (not shown) in a side face, a property is good by using the 1st and 2nd ceramic substrate 1 and 4, and since these ceramic substrates 1 and 4 have doubled the coefficient of thermal expansion, moreover, dimensional accuracy becomes good what has a short production process. Moreover, the engine performance of an inductor can be performed with a good thing because the ratio of the thickness to the line breadth of the inductor electrode 2 thickened thickness exceeding 0.3. moreover, the capacitor which puts the dielectric layer 6 of the 2nd ceramic substrate 4 -- the effect of a substrate, a glass layer, and the dielectric layer 6 on the electrode itself can be controlled by having added the glass frit which sets a conductor to 10 micrometers or more at least, forms the thickness after baking in the size which does not become smaller than the pattern size of a dielectric layer 6, and consists of a HOU lead silicate. Moreover, in order to carry out the debinder of the adhesion glass layer 8 for pasting up said the 1st ceramic substrate 1 and said 2nd ceramic substrate 4 before adhesion, a void is hard to generate it. The reliable manufacture approach of solid-state composite part can be offered from the above thing.
[0047] (Gestalt 2 of operation) Below, the manufacture approach of the solid-state composite part of an example of the manufacture approach of the electronic parts of this invention is explained, referring to a drawing.
[0048] When structural drawing of solid-state composite part is shown in drawing 2 , the sectional view of a ferrite substrate is shown in (a). The inductor electrode top view which is a spiral conductor pattern when making it the piece of an individual is shown in (b). The ring-like electrode top view on the ferrite layer when making it the piece of an individual is shown in (c). The sectional view of a forsterite substrate is shown in (d). The sectional view at the time of making a ferrite substrate and a forsterite substrate rival is shown in (e). The divided substrate sectional view is shown in (f). The inductor electrode 12 is first formed on the ferrite substrate 11, the ferrite layer 13 is formed on it, and the ring-like electrode 14 is formed on it. The capacitor which consists of the glass layer 16, the capacitor lower electrode 17, a dielectric layer 18, and a capacitor up electrode 19 is formed on the forsterite substrate 15, it pastes up on both sides of the adhesion glass layer 20, and the ferrite substrate 11 and the forsterite substrate 15 are cut to the piece of an individual after that.
[0049] The manufacture approach is explained below. On the ferrite substrate 11, the pattern of the inductor electrode 12 was formed by the intaglio imprint using the paste of silver and palladium, the substrate which performed pattern formation was calcinated by the peak temperature of 850 degrees C, and 10-minute maintenance, and the inductor electrode 12 was formed. At this time, the ratio of the thickness to the line breadth of the inductor electrode 12 was set to 0.8. Said inductor electrode 12 was formed upwards, a ferrite paste is used, the pattern of the ferrite layer 13 is formed by screen-stencil, it calcinates in 950 degrees C and 3 hours, and the ferrite layer 13 is formed. On said ferrite layer 13, the pattern of the ring-like electrode 14 was formed by screen-stencil using the paste of silver and palladium, the substrate which performed pattern formation was calcinated by the peak temperature of 850 degrees C, and 10-minute maintenance, and the ring-like electrode 14 was formed. Next, on the forsterite substrate 15 with the almost

same coefficient of thermal expansion as said ferrite substrate 11, the pattern of the glass layer 16 is formed by screen-stencil using the glass paste which consists of hoe silicic acid titanium, it calcinates by the peak temperature of 900 degrees C, and 10-minute keeping, and the glass layer 16 is formed. And the pattern of the capacitor lower electrode 17 is formed by screen-stencil on the glass layer 16 with the silver and the palladium paste which added the glass frit which consists of hoe aluminum silicate, and the pattern of the capacitor up electrode 19 is formed by screen-stencil on the capacitor lower electrode 17 using a dielectric paste with the silver and the palladium paste which formed by screen-stencil and used the pattern of a dielectric layer 18 for the lower electrode on the dielectric layer 18. This substrate is calcinated by the peak temperature of 850 degrees C, and 10-minute keeping, and a capacitor is formed. At this time, the pattern of the capacitor lower electrode 17 and the capacitor up electrode 19 was formed by the pattern which does not become smaller than a dielectric layer 18, and thickness could be 20 micrometers. Next, the pattern of the adhesion glass layer 20 was formed in the field which the inductor electrode 12 on the ferrite substrate 11 formed, and the field in which the capacitor of the forsterite substrate 15 was formed, by screen-stencil with a glass paste, and the debinder was performed in 500 degrees C and 30 minutes. And on both sides of the adhesion glass layer 20, lamination is performed for the ferrite substrate 11 and the forsterite substrate 15, a substrate is calcinated by the peak temperature of 700 degrees C, and 10-minute maintenance, and the ferrite substrate 11 and the forsterite substrate 15 are pasted up. After baking is completed, a substrate is cut to the piece of an individual and it becomes solid-state composite part by forming an external electrode (******) in a side face, and since substrates 11 and 15 have doubled the coefficient of thermal expansion, dimensional accuracy will become good. Moreover, even if it forms two or more inductor electrodes 14 into one component, the engine performance of an inductor can be made good, because the ratio of the thickness to the line breadth of the inductor electrode 12 thickened thickness exceeding 0.3, formed the non-magnetic material between patterns and formed the ring-like electrode 14 on the inductor electrode 12. moreover, the capacitor which forms the glass layer 16 which consists of hoe silicic acid titanium, and puts a dielectric layer 18 between the bottom of a capacitor -- the effect of a substrate, a glass layer, and the dielectric layer 18 on the electrode itself can be controlled by having added the glass frit which sets thickness to 10 micrometers or more, forms it in the size which does not become smaller than the pattern size of a dielectric layer 18, and consists a conductor of HOU aluminum silicate in it. Moreover, in order to carry out the debinder of the glass layer 16 for pasting up said ferrite substrate 11 and said forsterite substrate 15 before adhesion, a void is hard to generate it. The reliable manufacture approach of solid-state composite part can be offered from the above thing.

[0050] (Gestalt 3 of operation) Below, the manufacture approach of the solid-state composite part of an example of the manufacture approach of the electronic parts of this invention is explained, referring to a drawing.

[0051] When structural drawing of solid-state composite part is shown in drawing 3 , the sectional view of a ferrite substrate is shown in (a). The inductor electrode top view which is a spiral conductor pattern when making it the piece of an individual is shown in (b). The top view of the forsterite substrate in which the through tube was formed is shown in (c). The sectional view of a forsterite substrate is shown in (d). The sectional view at the time of making a ferrite substrate and a forsterite substrate rival is shown in (e). The divided substrate sectional view is shown in (f). First, the nonmagnetic glass layer 22 and the inductor electrode 23 are formed on the ferrite substrate 21, and the ferrite layer 24 is formed on these. After forming a through tube 26 in the forsterite substrate 25, the capacitor which consists of the capacitor lower electrode 27, a dielectric layer 28, and a capacitor up electrode 29 is formed on said forsterite substrate 25, it pastes up on both sides of the adhesion glass layer 30, and the ferrite substrate 21 and the forsterite substrate 25 are cut to the piece of an individual.

[0052] The manufacture approach is explained below. Formation is used on the ferrite substrate 21, a glass paste is used for this slot for a slot, the pattern of the nonmagnetic glass layer 22 is formed by screen-stencil, it calcinates in the peak temperature of 900 degrees C, and 10 minutes, and the glass layer 22 is formed. And by intaglio imprint, the pattern of the inductor electrode 23 was formed using the paste of silver and palladium, the substrate which performed pattern formation was calcinated by the peak temperature of 850 degrees C, and 10-minute maintenance, and the inductor electrode 23 was formed. At this time, the ratio of the thickness to the line breadth of the inductor electrode 23 was set to 1.5. Said inductor electrode 23 was formed upwards, a ferrite paste is used, the pattern of the ferrite layer 24 is formed by screen-stencil, it calcinates in 950 degrees C and 3 hours, and the ferrite layer 24 is formed. Next, on the forsterite substrate 25 with the almost same coefficient of thermal expansion as said ferrite substrate 21 in which the through tube 26 was formed The pattern of the capacitor lower electrode 27 is formed by screen-stencil with the silver and the platinum paste which added the glass frit which consists of a hoe calcium silicate. The pattern of a dielectric layer 28 is formed by screen-stencil on the capacitor lower electrode 27 using a dielectric paste, and the pattern of the capacitor up electrode 29 is formed by screen-stencil with the silver and the platinum paste used with the capacitor lower electrode 27 on the dielectric layer 28. This substrate is calcinated by the peak temperature of 900 degrees C, and 10-minute keeping, and a capacitor is formed. At this time, the pattern of the capacitor lower electrode 27 and the capacitor up electrode 29 was formed by the pattern which does not become smaller than a dielectric layer 28, and thickness could be 13 micrometers. Next, the pattern of the adhesion glass layer 30 was formed in the field in

which the inductor electrode 23 on the ferrite substrate 21 was formed, and the field in which the capacitor of the forsterite substrate 25 was formed, by screen-stencil with a glass paste, and the debinder was performed in 500 degrees C and 30 minutes. And on both sides of the adhesion glass layer 30, lamination is performed for the ferrite substrate 21 and the forsterite substrate 25, a substrate is calcinated by the peak temperature of 680 degrees C, and 10-minute maintenance, and the ferrite substrate 1 and the forsterite substrate 25 are pasted up. After baking is completed, a substrate is cut to the piece of an individual and it becomes solid-state composite part by forming an external electrode (not shown) in a side face, and since the ferrite substrate 21 and the forsterite substrate 25 have doubled the coefficient of thermal expansion, dimensional accuracy will become good. Moreover, the ratio of the thickness to the line breadth of the inductor electrode 23 thickens thickness exceeding 0.3, and by having formed in the slot between patterns the glass layer which is a non-magnetic material, even if it forms two or more inductor electrodes 23 into one component, the engine performance of an inductor can be made good. moreover, the capacitor which puts a dielectric layer 28 -- the effect of a substrate, a glass layer, and the dielectric layer 28 on the electrode itself can be controlled by having added the glass frit which sets thickness to 10 micrometers or more, forms it in the size which does not become smaller than the pattern size of a dielectric layer 28, and consists a conductor of a HOU calcium silicate in it. Moreover, the adhesion glass layer 30 for pasting up said ferrite substrate 21 and said forsterite substrate 25 is having formed the through tube 26 in the forsterite substrate 25 beforehand, since the occurring gas falls out to a through tube 26 at the time of baking of a glue line, does not generate a fine void, either but can acquire higher dependability. The reliable manufacture approach of solid-state composite part can be offered from the above thing.

[0053] (Gestalt 4 of operation) Below, the manufacture approach of the solid-state composite part of an example of the manufacture approach of the electronic parts of this invention is explained, referring to a drawing.

[0054] When structural drawing of solid-state composite part is shown in drawing 4 , the sectional view of a ferrite substrate is shown in (a). The inductor electrode top view which is a spiral conductor pattern when making it the piece of an individual is shown in (b). The sectional view of a forsterite substrate is shown in (c). The sectional view at the time of making a ferrite substrate and a forsterite substrate rival is shown in (d). The divided substrate sectional view is shown in (e). First, the inductor electrode 32, the ring-like electrode 33, and the nonmagnetic glass layer 34 are formed on the ferrite substrate 31, and the ferrite layer 35 is formed on these. The glass layer 37 is formed on the forsterite substrate 36, the capacitor which consists of the capacitor lower electrode 38, a dielectric layer 39, and a capacitor up electrode 40 is formed on said glass layer 37, it pastes up on both sides of the adhesion glass layer 41, and the ferrite substrate 31 and the forsterite substrate 36 are cut to the piece of an individual.

[0055] The manufacture approach is explained below. The pattern of the inductor electrode 32 and the ring-like electrode 33 was formed by intaglio imprint on the ferrite substrate 31 using the silver paste, the substrate which performed pattern formation was calcinated by the peak temperature of 900 degrees C, and 10-minute maintenance, and the inductor electrode 32 and the ring-like electrode 33 were formed. At this time, the ratio of the thickness to the line breadth of the inductor electrode 32 was set to 1.5. Moreover, said ring-like electrode 33 is connected by beer (not shown). On the substrate in which said electrode was formed, a glass paste is used, the pattern of the nonmagnetic glass layer 34 is formed by screen-stencil, it calcinates in the peak temperature of 900 degrees C, and 10 minutes, and the glass layer 34 is formed. Said inductor electrode 32 was formed upwards, a ferrite paste is used, the pattern of the ferrite layer 35 is formed by screen-stencil, it calcinates in 970 degrees C and 3 hours, and the ferrite layer 35 is formed. Next, on the forsterite substrate 36 with the almost same coefficient of thermal expansion as said ferrite substrate 31, the paste of boro-silicated glass is used, the pattern of the glass layer 37 is formed by screen-stencil, it calcinates by the peak temperature of 900 degrees C, and 10-minute keeping, and the glass layer 37 is formed. And the pattern of the capacitor lower electrode 38 is formed by screen-stencil on the glass layer 37 with the silver and the platinum paste which added the glass frit which consists of hoe silicic acid titanium, the pattern of a dielectric layer 39 is formed by screen-stencil on the capacitor lower electrode 38 using a dielectric paste, and the pattern of the capacitor up electrode 40 is formed by screen-stencil with the silver and the platinum paste used with the capacitor lower electrode 38 on the dielectric layer 39. This substrate is calcinated by the peak temperature of 900 degrees C, and 10-minute keeping, and a capacitor is formed. At this time, the pattern of the capacitor lower electrode 38 and the capacitor up electrode 40 was formed by the pattern which does not become smaller than a dielectric layer 39, and thickness could be 13 micrometers. Next, the pattern of the adhesion glass layer 41 was formed in the field in which the inductor electrode 32 on the ferrite substrate 31 was formed, and the field in which the capacitor of the forsterite substrate 36 was formed, by screen-stencil with a glass paste, and the debinder was performed in 500 degrees C and 30 minutes. And on both sides of the adhesion glass layer 41, lamination is performed for the ferrite substrate 31 and the forsterite substrate 36, a substrate is calcinated by the peak temperature of 730 degrees C, and 10-minute maintenance, and the ferrite substrate 31 and the forsterite substrate 36 are pasted up. After baking is completed, a substrate is cut to the piece of an individual and it becomes solid-state composite part by forming an external electrode (not shown) in a side face.

[0056] In addition, since substrates 31 and 36 have doubled the coefficient of thermal expansion, dimensional

accuracy will become good. Moreover, by the ratio of the thickness to the line breadth of the inductor electrode 32 having thickened thickness exceeding 0.3, having formed the glass layer which is a non-magnetic material between patterns, and having formed the ring-like electrode 33 around inductor electrode 32, even if it forms two or more inductor electrodes 32 into one component, the engine performance of an inductor can be made good. moreover, the capacitor which forms the boro-silicated glass layer 37 in the bottom of a capacitor, and puts a dielectric layer 39 -- the effect of a substrate, a glass layer, and the dielectric layer 39 on the electrode itself can be controlled by having added the glass frit which sets thickness to 10 micrometers or more, forms it in the size which does not become smaller than the pattern size of a dielectric layer 39, and consists a conductor of hoe silicic acid titanium in it. The reliable manufacture approach of solid-state composite part can be offered from the above thing.

[0057] In addition, although the example of the gestalt of four operations explained in the above explanation, in a wiring substrate which needs electrode wiring which makes a coefficient of thermal expansion almost the same, it can carry out similarly. Furthermore, although a spiral conductor pattern is the thing of a monolayer and is performed with the above-mentioned operation gestalt, even if it forms in two or more layers, the same solid-state composite part is obtained. Moreover, a spiral conductor pattern can be similarly carried out, if it is the wiring electrode pattern of a configuration of that it can be used as an inductor electrode.

[0058] Moreover, even if it carries out grinding at least of one side and makes substrate thickness thin after joining the 1st and 2nd ceramic substrate by the glue line, the same solid-state composite part is obtained. a capacitor -- although it is four kinds of things and being explained to the glass frit used for a conductor, if it becomes, it will be the thing which is the glass frit which consists of hoe silicic acid, a hoe lead silicate, a hoe calcium silicate, hoe aluminum silicate, hoe silicic acid titanium, mixture, or a compound and from which the same effectiveness is acquired. Moreover, although the glass layers formed in the bottom of a capacitor are two kinds of things and are explained, the same effectiveness will be acquired if it is the glass frit which consists of hoe silicic acid, a hoe lead silicate, a hoe calcium silicate, hoe aluminum silicate, hoe silicic acid titanium, mixture, or a compound.

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[Translation done.]

## DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] (a) is the sectional view showing the structure of the 1st ceramic substrate in the manufacture approach of the solid-state composite part of the gestalt 1 operation of this invention.
(b) -- said -- the top view of the inductor electrode pattern when making it the piece of an individual on the 1st ceramic substrate
(c) is the sectional view showing the structure of this 2nd ceramic substrate.
(d) is a sectional view when unifying this 1st ceramic substrate and the 2nd ceramic substrate through a glue line.
(e) is a sectional view when cutting this solid-state composite part.
[Drawing 2] (a) is the sectional view showing the structure of the ferrite substrate in the manufacture approach of the solid-state composite part of the gestalt other operations of this invention.
(b) is the top view of the inductor electrode pattern when making it the piece of an individual on this ferrite substrate.
(c) is the top view of the ring-like electrode pattern of the shape of a ferrite layer of this ferrite substrate.
(d) is the sectional view showing the structure of this forsterite substrate.
(e) is a sectional view when unifying this ferrite substrate and a forsterite substrate through a glue line.
(f) is a sectional view when cutting this solid-state composite part.
[Drawing 3] (a) is the sectional view showing the structure of a ferrite substrate [ in / further / the manufacture approach of the solid-state composite part of the gestalt other operations ] of this invention.
(b) is the top view of the inductor electrode pattern when making it the piece of an individual on this ferrite substrate.
(c) is the top view of the forsterite substrate in which this through tube was formed.
(d) is the sectional view showing the structure of this forsterite substrate.
(e) is a sectional view when unifying this ferrite substrate and a forsterite substrate through a glue line.
(f) is a sectional view when cutting this solid-state composite part.
[Drawing 4] (a) is the sectional view showing the structure of the ferrite substrate in the manufacture approach of the solid-state composite part of the gestalt 1 operation of this invention.
(b) is the top view of the inductor electrode pattern when making it the piece of an individual on this ferrite substrate.
(c) is the sectional view showing the structure of this forsterite substrate.
(d) is a sectional view when unifying this ferrite substrate and a forsterite substrate through a glue line.
(e) is a sectional view when cutting this solid-state composite part.
[Description of Notations]
1 1st Ceramic Substrate
2 Inductor Electrode
3 Ferrite Layer
4 2nd Ceramic Substrate
5 Capacitor Lower Electrode
6 Dielectric Layer
7 Capacitor Up Electrode
8 Adhesion Glass Layer
11 Ferrite Substrate
12 Inductor Electrode
13 Ferrite Layer
14 Ring-like Electrode
15 Forsterite Substrate
16 Glass Layer
17 Capacitor Lower Electrode
18 Dielectric Layer
19 Capacitor Up Electrode

20 Adhesion Glass Layer
21 Ferrite Substrate
22 Nonmagnetic Glass Layer
23 Inductor Electrode
24 Ferrite Layer
25 Forsterite Substrate
26 Through Tube
27 Capacitor Lower Electrode
28 Dielectric Layer
29 Capacitor Up Electrode
30 Adhesion Glass Layer
31 Ferrite Substrate
32 Inductor Electrode
33 Ring-like Electrode
34 Nonmagnetic Glass Layer
35 Ferrite Layer
36 Forsterite Substrate
37 Glass Layer
38 Capacitor Lower Electrode
39 Dielectric Layer
40 Capacitor Up Electrode
41 Adhesion Glass Layer

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[Translation done.]

* NOTICES *



1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

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DRAWINGS

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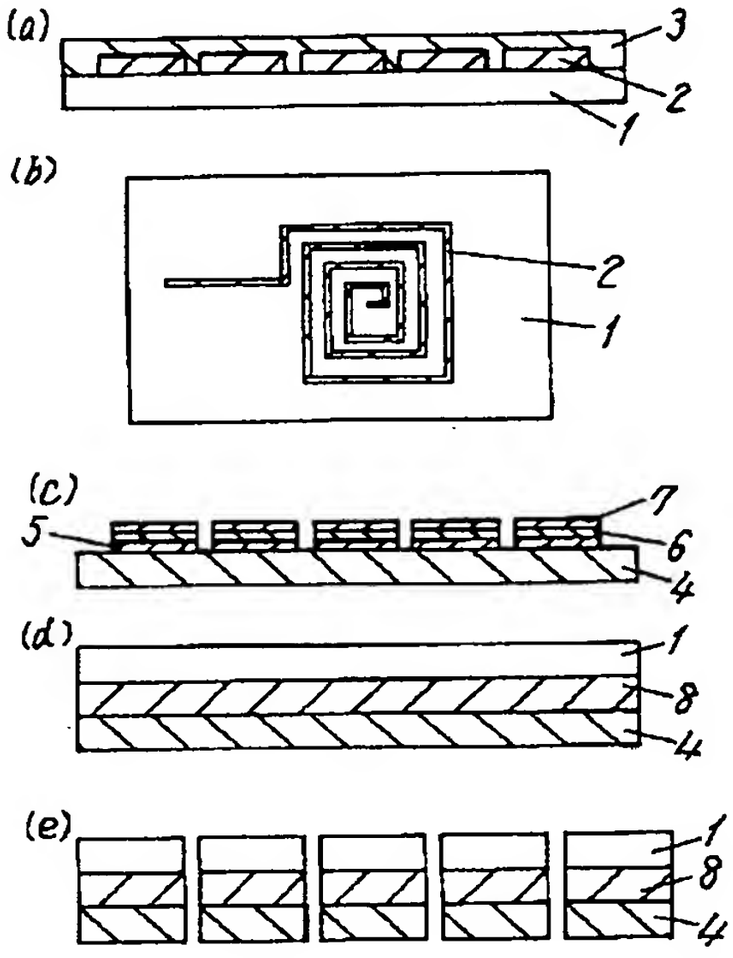
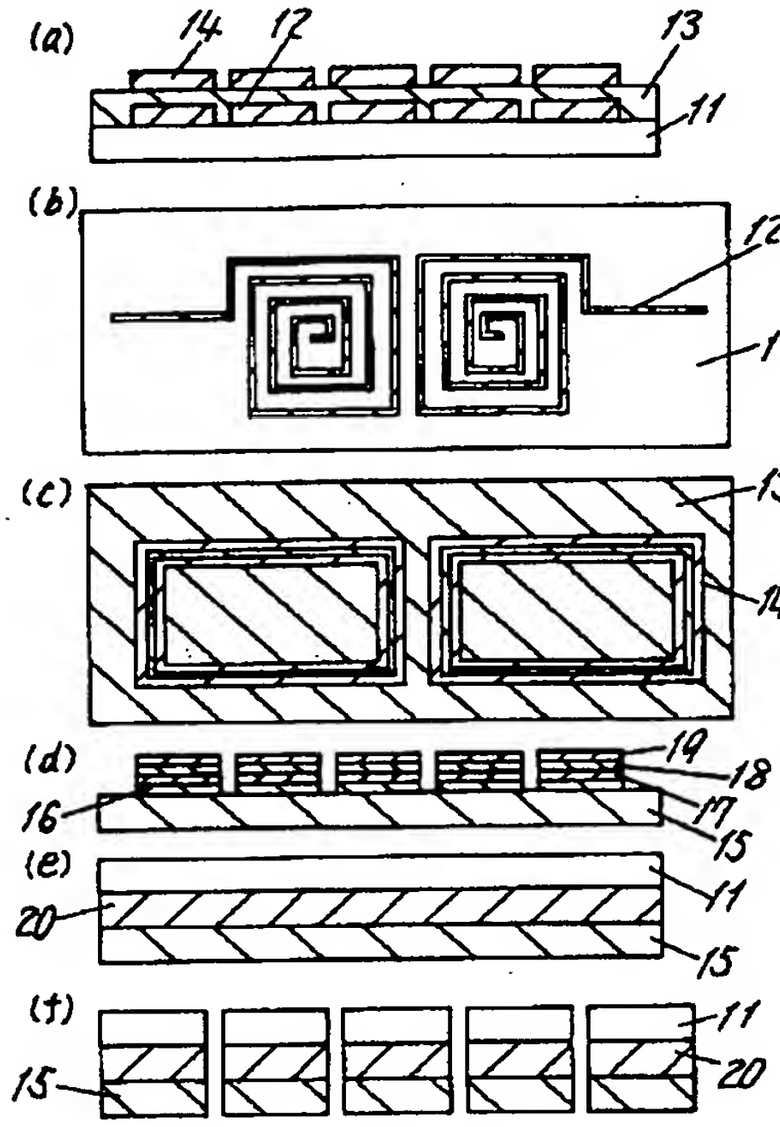
[Drawing 1]

1 第1のセラミック基板　5 コンデンサ下部電極
2 インタクタ電極　6 誘電体層
3 フェライト層　7 コンデンサ上部電極
4 第2のセラミック基板　8 接着ガラス層



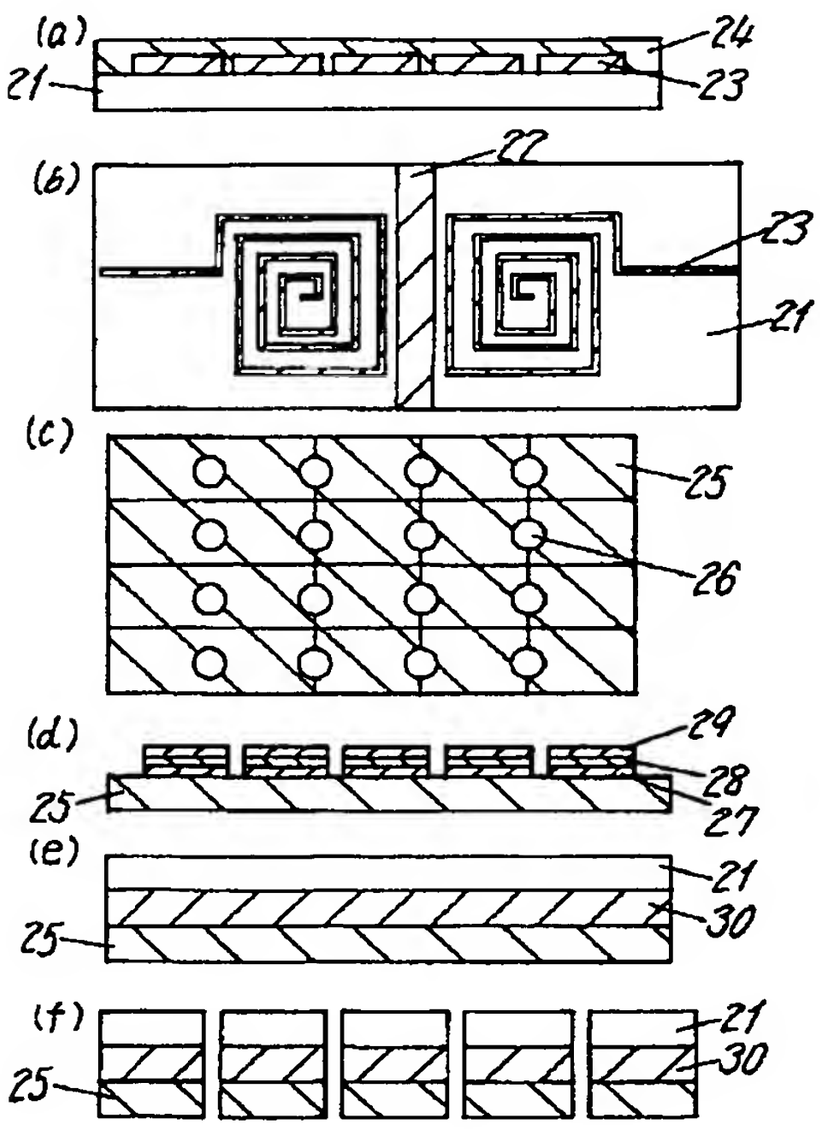

[Drawing 2]

11 フェライト基板　16 ガラス層
12 インダクタ電極　17 コンデンサ下部電極
13 フェライト層　18 誘電体層
14 リング状電極　19 コンデンサ上部電極
15 フォルステライト基板　20 接着ガラス層



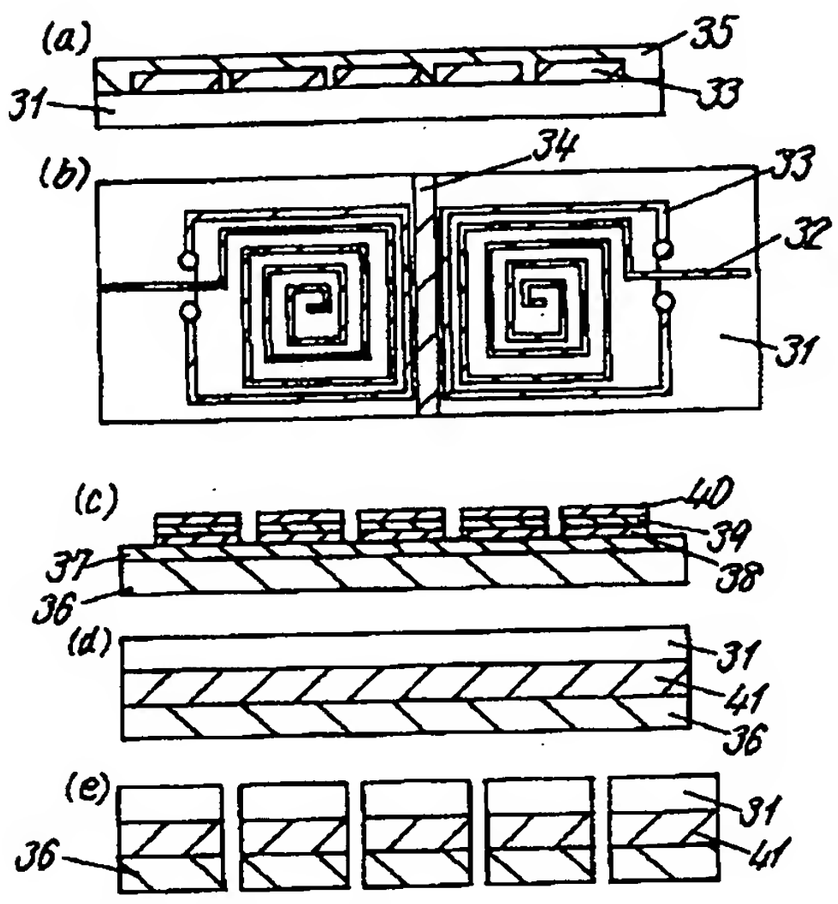

[Drawing 3]

21 フェライト基板　26 貫通孔
22 非磁性ガラス層　27 コンデンサ下部電極
23 インダクタ電極　28 誘電体層
24 フェライト層　29 コンデンサ上部電極
25 フォルステライト基板　30 接着ガラス層




[Drawing 4]

31 フェライト基板
32 インダクタ電極
33 リング状電極
34 非磁性ガラス層
35 フェライト層
36 フォルステライト基板
37 ガラス層
38 コンデンサ下部電極
39 誘電体層
40 コンデンサ上部電極
41 接着ガラス層

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[Translation done.]

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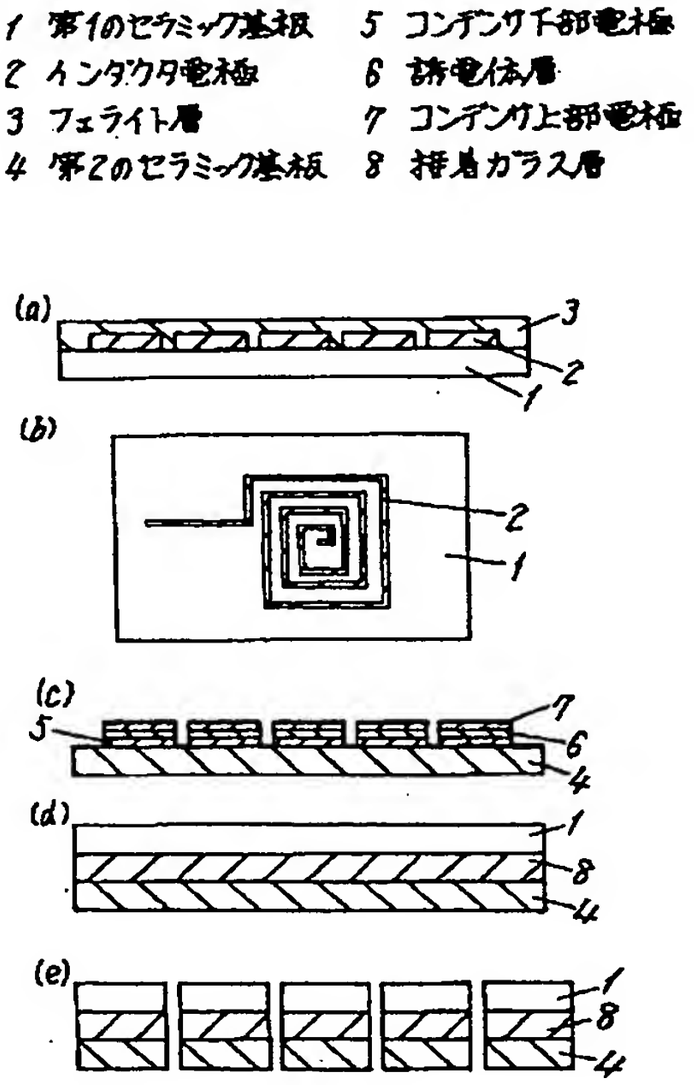
最終頁に続く

(54)【発明の名称】　固体複合部品の製造方法

(57)【要約】
【課題】　寸法精度がよく、かつ信頼性が高い小型化の固体複合部品の製造方法を提供することを目的とする。
【解決手段】　第1の未焼成セラミック基板および第2の未焼成セラミック基板を焼成して、第1のセラミック基板1および第2のセラミック基板4を形成し、この第1のセラミック基板1上には、インダクタ導体パターン層として、インダクタ電極2を形成し、その上に磁性ペースト層としてフェライト層3を形成して、インダクタ層を設け、第2のセラミック基板4上には、コンデンサ導体パターン層として、コンデンサ下部電極5、コンデンサ上部電極7、および誘電体層6からなるコンデンサ層を設け、第1、第2のセラミック基板の少なくとも一方にガラスペースト層として接着ガラス層8を塗布し、互いに張り合わせて張合体を形成し、この張合体を焼成して焼成体を形成し、この焼成体に外部電極を形成する。



【特許請求の範囲】

【請求項1】　第1のセラミック基板の一面上にインダクタ導体パターン層を形成するとともに、前記インダクタ導体パターン層上に磁性ペースト層を形成してインダクタ層を有した第1の基板を形成する第1工程と、第2のセラミック基板の一面上に誘電体層を介在したコンデンサ導体パターン層を形成してコンデンサ層を有した第2の基板を形成する第2工程と、前記第1の基板の一面側または前記第2の基板の一面側の少なくとも一方に、ガラスペースト層を形成するとともに、前記第1の基板および前記第2の基板を前記ガラスペースト層を介して互いに張り合わせて張合体を形成する第3工程と、前記張合体を焼成して焼成体を形成する第4工程と、前記焼成体に外部電極を形成する第5工程とを備え、前記第1工程前に、第1の未焼成セラミック基板および第2の未焼成セラミック基板を焼成して第1のセラミック基板および第2のセラミック基板を形成する工程を設けた固体複合部品の製造方法。

【請求項2】　第1工程の、インダクタ導体パターン層は、可撓性樹脂基板からなる凹版の表面に設けたパターン溝に導電性ペーストを充填し乾燥する工程と、前記凹版と第1のセラミック基板の一面とを加熱および加圧しながら張り合わせる工程と、前記凹版を前記第1のセラミック基板から剥離して前記導電性ペーストを前記第1のセラミック基板上に転写する工程と、前記第1のセラミック基板を焼成する工程とを有する請求項1記載の固体複合部品の製造方法。

【請求項3】　第2の工程において、第2のセラミック基板とコンデンサ層との間にガラスペースト層の中間層を形成する工程を設けた請求項1記載の固体複合部品の製造方法。

【請求項4】　ガラスペースト層の材質を、ホウ珪酸、ホウ珪酸鉛、ホウ珪酸カルシウム、ホウ珪酸アルミニウム、ホウ珪酸チタンのいずれか一つ、またはその混合物、またはその化合物からなるガラスフリットを有した材質とした請求項3記載の固体複合部品の製造方法。

【請求項5】　第3工程において、ガラスペースト層を形成した後に脱バインダする工程を設けた請求項1記載の固体複合部品の製造方法。

【請求項6】　第4工程前に、第2のセラミック基板に複数個の貫通孔を形成するとともに、前記貫通孔に銀電極を形成する工程を設け、第4工程後に焼成体を個片に分割し前記銀電極が側面に表出するように焼成個片体を形成する工程を設け、第5工程において前記銀電極で外部電極に形成する工程を設けた請求項1記載の固体複合部品の製造方法。

【請求項7】　第4工程後に、焼成体を個片に分割し焼成個片体を形成する工程を設けた請求項1記載の固体複合部品の製造方法。

【請求項8】　第4工程後に、第1のセラミック基板または第2のセラミック基板の少なくとも一方を研削し、第1のセラミック基板または第2のセラミック基板の少なくとも一方の基板厚を薄くする工程を設けた請求項1記載の固体複合部品の製造方法。

【請求項9】　第1のセラミック基板および第2のセラミック基板は、熱膨張係数を互いに同等にした請求項1記載の固体複合部品の製造方法。

【請求項１０】　第1のセラミック基板の材質をフェライトを有した材質とし、第2のセラミック基板の材質をフォルステライトを有した材質とした請求項9記載の固体複合部品の製造方法。

【請求項１１】　コンデンサ導体パターン層の面積を誘電体層の面積よりも大きくした請求項1記載の固体複合部品の製造方法。

【請求項１２】　コンデンサ導体パターン層の材質を、ホウ珪酸、ホウ珪酸鉛、ホウ珪酸カルシウム、ホウ珪酸アルミニウム、ホウ珪酸チタンのいずれか一つ、またはその混合物、またはその化合物からなるガラスフリットを有した材質とした請求項1記載の固体複合部品の製造方法。

【請求項１３】　インダクタ導体パターン層を複数層形成する工程を設けた請求項1記載の固体複合部品の製造方法。

【請求項１４】　インダクタ導体パターン層は、線状導体を渦巻状にした渦巻状導体部を有し、前記渦巻状導体部の前記線状導体は、導体幅に対する導体厚比を０．３を越えるようにした請求項1記載の固体複合部品の製造方法。

【請求項１５】　インダクタ導体パターン層は、線状導体を渦巻状にした渦巻状導体部を少なくとも２個有し、隣接する前記渦巻状導体部間線上に、非磁性材料を形成する工程を設けた請求項1記載の固体複合部品の製造方法。

【請求項１６】　インダクタ導体パターン層は、線状導体を渦巻状にした渦巻状導体部を少なくとも２個有し、隣接する前記渦巻状導体部間線上に、非磁性材料を形成するとともに、前記渦巻状導体部間線上の第1のセラミック基板に溝を形成し、前記溝にも前記非磁性材料を形成する工程を設けた請求項1記載の固体複合部品の製造方法。

【請求項１７】　インダクタ導体パターン層は、線状導体を渦巻状にした渦巻状導体部と、線状導体をリング状にしたリング状導体部とを有し、前記渦巻状導体部の外側に前記リング状導体部を形成する工程を設けた請求項1記載の固体複合部品の製造方法。

【請求項１８】　インダクタ導体パターン層は、線状導体を渦巻状にした渦巻状導体部と、線状導体をリング状にしたリング状導体部とを有し、前記渦巻状導体部の外側に前記リング状導体部を形成するとともに、前記リング状導体部を磁性ペースト層中に形成する工程を設けた

請求項1 記載の固体複合部品の製造方法。
【 請求項１９】 リング状導体部をアース接続する工程を設けた請求項１７記載の固体複合部品の製造方法。
【 請求項２０】 渦巻状導体部とリング状導体部とを同時に同一平面上に形成する工程を設けた請求項１７記載の固体複合部品の製造方法。
【 発明の詳細な説明】
【０００１】
【 発明の属する技術分野】本発明は、インダクタ、キャパシタ等が複合したチップ型の固体複合部品の製造方法に関するものである。
【０００２】
【 従来の技術】近年、半導体ＬＳＩ、チップ部品等は小型、軽量化が進んでおり、この中で高周波関連の磁気デバイスでも小型化の要求があり、厚膜の誘電体を使用したコンデンサの小型化の要求が多くなり、１つのデバイスの中に誘電体とインダクタを一体化にして小型にする方法などが開発されてきている。
【０００３】小型化を図ったコンデンサ形成方法では、特公平2 －５４６４７号公報において、非磁性絶縁体層とコンデンサ用電極導体とを交互積層し、その上に更に同じ材質の非磁性絶縁体層とコイル用導体とを交互積層し、これらを一体焼成してインダクタとコンデンサを複合化して小型化を図る方法が紹介されている。またより簡便な固体複合部品の製造方法として、特開昭５７－１９３０１９号公報に開示されているように、磁性体シートと、誘電体シートを焼成し、中間層で貼り合わせ一体化するという方法が紹介されている。
【０００４】
【 発明が解決しようとする課題】上記従来の方法では、インダクタとコンデンサを一体焼成するには、磁性体シートと、誘電体シート共に、低温焼結材を使用する必要があり、特性向上を図りにくい。また、磁性体シートと、誘電体シートの熱膨張係数の違いから、焼成時において収縮率が異なり、寸法精度の向上も図りにくいという問題点を有していた。
【０００５】本発明は上記問題点を解決し、特性向上および寸法精度の向上を図った固体複合部品の製造方法を提供することを目的としている。
【０００６】
【 課題を解決するための手段】上記問題点を解決するために本発明は、第1 のセラミック基板の一面上に、インダクタ導体パターン層を形成するとともに、前記インダクタ導体パターン層上に磁性ペースト層を形成して、インダクタ層を有した第1 の基板を形成する第1 工程と、第2 のセラミック基板の一面上に誘電体層を介在したコンデンサ導体パターン層を形成して、コンデンサ層を有した第2 の基板を形成する第2 工程と、前記第1 の基板の一面側または前記第2 の基板の一面側の少なくとも一方に、ガラスペースト層を形成するとともに、前記第1 の基板および前記第2 の基板を前記ガラスペースト層を介して互いに張り合わせて張合体を形成する第3 工程と、前記張合体を焼成して、焼成体を形成する第4 工程と、前記焼成体に外部電極を形成する第5 工程とを備え、前記第1 工程前に、第1 の未焼成セラミック基板および第2 の未焼成セラミック基板を焼成して、第1 のセラミック基板および第2 のセラミック基板を形成する工程を設けた製造方法である。
【０００７】上記製造方法により、インダクタ層およびコンデンサ層はセラミック基板上に形成するので、特性向上を図ることができる。
【０００８】さらに、第1 のセラミック基板および第2 のセラミック基板は、未焼成のセラミック基板である第1 の未焼成セラミック基板および第2 の未焼成セラミック基板を焼成して形成しているので、張合体を焼成して焼成体を形成する際に、第1 のセラミック基板および第2 のセラミック基板が、全体的に熱収縮することがない。これにより、第1 、第2 のセラミック基板上に形成したインダクタ層およびコンデンサ層が、第1 、第2 のセラミック基板の収縮に合わせて、収縮してしまうことがなく、寸法精度を向上させることができるとともに、後工程等において、寸法を調整する必要もなく、製造工程を簡略化することもできる。
【０００９】
【 発明の実施の形態】本発明の請求項1 記載の発明は、第1 のセラミック基板の一面上に、インダクタ導体パターン層を形成するとともに、前記インダクタ導体パターン層上に磁性ペースト層を形成して、インダクタ層を有した第1 の基板を形成する第1 工程と、第2 のセラミック基板の一面上に誘電体層を介在したコンデンサ導体パターン層を形成して、コンデンサ層を有した第2 の基板を形成する第2 工程と、前記第1 の基板の一面側または前記第2 の基板の一面側の少なくとも一方に、ガラスペースト層を形成するとともに、前記第1 の基板および前記第2 の基板を前記ガラスペースト層を介して互いに張り合わせて張合体を形成する第3 工程と、前記張合体を焼成して、焼成体を形成する第4 工程と、前記焼成体に外部電極を形成する第5 工程とを備え、前記第1 工程前に、第1 の未焼成セラミック基板および第2 の未焼成セラミック基板を焼成して、第1 のセラミック基板および第2 のセラミック基板を形成する工程を設けた製造方法である。
【００１０】上記製造方法により、インダクタ層およびコンデンサ層はセラミック基板上に形成するので、特性向上を図ることができる。
【００１１】さらに、第1 のセラミック基板および第2 のセラミック基板は、未焼成のセラミック基板である第1 の未焼成セラミック基板および第2 の未焼成セラミック基板を焼成して形成しているので、張合体を焼成して焼成体を形成する際に、第1 のセラミック基板および第

2のセラミック基板が、全体的に熱収縮することがない。これにより、第1、第2のセラミック基板上に形成したインダクタ層およびコンデンサ層が、第1、第2のセラミック基板の収縮に合わせて、収縮してしまうことがなく、寸法精度を向上させることができるとともに、後工程等において、寸法を調整する必要もなく、製造工程を簡略化することもできる。

【００１２】本発明の請求項2記載の発明は、請求項1記載の発明において、第1工程は、インダクタ導体パターン層は、可撓性樹脂基板からなる凹版の表面に設けたパターン溝に、導電性ペーストを充填し乾燥する工程と、前記凹版と第1のセラミック基板の一面とを、加熱および加圧しながら張り合わせる工程と、前記凹版を前記第1のセラミック基板から剥離して、前記導電性ペーストを前記第1のセラミック基板上に転写する工程と、前記第1のセラミック基板を焼成する工程とを有して形成した製造方法である。

【００１３】上記製造方法により、パターン形状の良い、ファインな配線で、かつ膜厚の厚いインダクタ導体パターン層を形成することができる。

【００１４】本発明の請求項3記載の発明は、請求項1記載の発明の第2の工程において、第2のセラミック基板とコンデンサ層との間にガラスペースト層の中間層を形成する工程を設けた製造方法である。

【００１５】上記製造方法により、第2のセラミック基板とコンデンサ層との間にガラスペースト層の中間層を形成しているので、コンデンサ層への第2の基板からの影響を抑制することができる。

【００１６】本発明の請求項4記載の発明は、請求項3記載の発明において、ガラスペースト層の材質を、ホウ珪酸、ホウ珪酸鉛、ホウ珪酸カルシウム、ホウ珪酸アルミニウム、ホウ珪酸チタンのいずれか一つ、またはその混合物、またはその化合物からなるガラスフリットを有した材質とした製造方法である。

【００１７】上記製造方法により、コンデンサ層への第2のセラミック基板からの影響を抑制することができる。

【００１８】本発明の請求項5記載の発明は、請求項1記載の発明において、第3工程において、ガラスペースト層を形成した後に、脱バインダする工程を設けた請求項1記載の固体複合部品の製造方法である。

【００１９】上記製造方法により、ガラスペースト層を形成した後に、脱バインダする工程を設けているので、ボイドが発生せず、信頼性を向上させることができる。

【００２０】本発明の請求項6記載の発明は、請求項1記載の発明において、第4工程前に、第2のセラミック基板に複数個の貫通孔を形成するとともに、前記貫通孔に銀電極を形成する工程を設け、第4工程後に、焼成体を個片に分割し、前記銀電極が側面に表出するように、焼成個片体を形成する工程を設け、第5工程において、前記銀電極により外部電極に形成する工程を設けた製造方法である。

【００２１】上記製造方法により、第2のセラミック基板に貫通孔を形成するので、張合体の焼成時に、ガラスペースト層の中間層から発生するガスが貫通孔から抜けるので、細かいボイドも発生せず、信頼性を非常に向上させることができる。

【００２２】本発明の請求項7記載の発明は、請求項1記載の発明において、第4工程後に、焼成体を個片に分割し、焼成個片体を形成する工程を設けた製造方法である。

【００２３】上記製造方法により、大量生産を効率よくすることができる。本発明の請求項8記載の発明は、請求項1記載の発明において、第4工程後に、第1のセラミック基板または第2のセラミック基板の少なくとも一方を研削し、第1のセラミック基板または第2のセラミック基板の少なくとも一方の基板厚を薄くする工程を設けた製造方法である。

【００２４】上記製造方法により、薄型化を図ることができる。本発明の請求項9記載の発明は、請求項1記載の発明において、第1のセラミック基板および第2のセラミック基板は、熱膨張係数を互いに同等にした製造方法である。

【００２５】上記製造方法により、第1のセラミック基板および第2のセラミック基板の熱膨張係数を互いに同等にしているので、張合体の焼成時における第1、第2のセラミック基板の膨張率が等しくなるので、歪み等が生じず、寸法精度を向上させることができる。

【００２６】本発明の請求項10記載の発明は、請求項9記載の発明において、第1のセラミック基板の材質をフェライトを有した材質とし、第2のセラミック基板の材質をフォルステライトを有した材質とした製造方法である。

【００２７】上記製造方法により、良好な性能を得ることができる。本発明の請求項11記載の発明は、請求項1記載の発明において、コンデンサ導体パターン層の面積を誘電体層の面積よりも大きくした製造方法である。

【００２８】上記製造方法により、コンデンサ層への第2のセラミック基板、ガラスペースト層の中間層からの影響を抑制することができる。

【００２９】本発明の請求項12記載の発明は、請求項1記載の発明において、コンデンサ導体パターン層の材質を、ホウ珪酸、ホウ珪酸鉛、ホウ珪酸カルシウム、ホウ珪酸アルミニウム、ホウ珪酸チタンのいずれか一つ、またはその混合物、またはその化合物からなるガラスフリットを有した材質とした製造方法である。

【００３０】上記製造方法により、コンデンサ導体パターン層の誘電体への影響を抑制することができる。

【００３１】本発明の請求項13記載の発明は、請求項1記載の発明において、インダクタ導体パターン層を複

数層形成する工程を有した製造方法である。

【００３２】上記製造方法により、良好なインダクタ層を形成することができる。本発明の請求項１４記載の発明は、請求項1記載の発明において、インダクタ導体パターン層は、線状導体を渦巻状にした渦巻状導体部を有し、前記渦巻状導体部の前記線状導体は、導体幅に対する導体厚比を０．３を越えるようにした製造方法である。

【００３３】上記製造方法により、渦巻状導体部の厚さが厚くなるので、インダクタ性能を良好にすることができる。

【００３４】本発明の請求項１５記載の発明は、請求項１記載の発明において、インダクタ導体パターン層は、線状導体を渦巻状にした渦巻状導体部を少なくとも２個有し、隣接する前記渦巻状導体部間線上に、非磁性材料を形成する工程を設けた製造方法である。

【００３５】上記製造方法により、インダクタ性能を高性能にすることができる。本発明の請求項１６記載の発明は、請求項1記載の発明において、インダクタ導体パターン層は、線状導体を渦巻状にした渦巻状導体部を少なくとも２個有し、隣接する前記渦巻状導体部間線上に、非磁性材料を形成するとともに、前記渦巻状導体部間線上の第1のセラミック基板に溝を形成し、前記溝にも前記非磁性材料を形成する工程を設けた製造方法である。

【００３６】上記製造方法により、インダクタ性能を高性能にすることができる。本発明の請求項１７記載の発明は、請求項1記載の発明において、インダクタ導体パターン層は、線状導体を渦巻状にした渦巻状導体部と、線状導体をリング状にしたリング状導体部とを有し、前記渦巻状導体部の外側に前記リング状導体部を形成する工程を設けた製造方法である。

【００３７】上記製造方法により、渦巻状導体部によるインダクタンスに逆磁界が発生作用して、周波数特性が延び、高周波領域でも良好な減衰量を得ることができる。

【００３８】本発明の請求項１８記載の発明は、請求項１記載の発明において、インダクタ導体パターン層は、線状導体を渦巻状にした渦巻状導体部と、線状導体をリング状にしたリング状導体部とを有し、前記渦巻状導体部の外側に前記リング状導体部を形成するとともに、前記リング状導体部を磁性ペースト層中に形成する工程を設けた製造方法である。

【００３９】上記製造方法により、リング状導体部を磁性ペースト層中に形成するので、より一層、渦巻状導体部によるインダクタンスに逆磁界が発生作用して、周波数特性が延び、高周波領域でも良好な減衰量を得ることができる。

【００４０】本発明の請求項１９記載の発明は、請求項１７記載の発明において、リング状導体部をアース接続する工程を設けた製造方法である。

【００４１】上記製造方法により、高周波領域で良好な減衰量を得ることができる。本発明の請求項２０記載の発明は、請求項１７記載の発明において、渦巻状導体部とリング状導体部とを同時に同一平面上に形成する工程を設けた製造方法である。

【００４２】上記製造方法により、製造工程を簡略化することができる。

（実施の形態１）以下に、本発明の一実施の形態における固体複合部品の製造方法について、図面を参照しながら説明する。

【００４３】図1において、固体複合部品の構造図を示すと、（ａ）には第1のセラミック基板の断面図を示す。（ｂ）には個片にした時の渦巻状導体パターンであるインダクタ電極平面図を示す。（ｃ）には第2のセラミック基板の断面図を示す。（ｄ）には第1、第2のセラミック基板を張り合わせた時の断面図を示す。（ｅ）には分割したセラミック基板断面図を示す。

【００４４】第1の未焼成セラミック基板および第2の未焼成セラミック基板を焼成して、第1のセラミック基板1および第2のセラミック基板4を形成する。この第1のセラミック基板1上には、インダクタ導体パターン層として、インダクタ電極2を形成し、その上に、磁性ペースト層として、フェライト層3を形成して、インダクタ層を設ける。第2のセラミック基板4上には、コンデンサ導体パターン層として、コンデンサ下部電極5、コンデンサ上部電極7、および誘電体層6からなるコンデンサ層を設け、第1、第2のセラミック基板１，４の少なくとも一方にガラスペースト層として接着ガラス層８を塗布して、互いに張り合わせ、張合体を形成し、この張合体を焼成して、焼成体を形成し、この焼成体に外部電極を形成している。

【００４５】また、インダクタ電極2は、線状導体を渦巻状にした渦巻状導体部により形成している。

【００４６】以下に製造方法を説明する。セラミック基板1上に、凹版転写にて銀のペーストを使用してインダクタ電極2のパターンを形成し、パターン形成を行った基板をピーク温度８５０℃、１０分保持で焼成を行い、インダクタ電極2を形成した。この時インダクタ電極2の線幅に対する膜厚の比は０．４とした。前記インダクタ電極2上にフェライトペーストでフェライト層3のパターンをスクリーン印刷で形成を行い、パターン形成を行った基板を９３０℃、２時間で焼成を行い、フェライト層3を形成した。次に、第1のセラミック基板1とほぼ同じ熱膨張係数を持つ第2のセラミック基板4上に、ホウ珪酸鉛からなるガラスフリットを添加したＡｇペーストでコンデンサ下部電極5のパターンをスクリーン印刷で形成し、コンデンサ下部電極5上に誘電体ペーストを使用して誘電体層6のパターンをスクリーン印刷し、誘電体層6上に下部電極に用いたＡｇペーストによりコ

ンデンサ上部電極7 のパターンをスクリーン印刷で形成する。この基板をピーク温度９００℃、１０分キープで焼成を行いコンデンサを形成する。この時コンデンサ下部電極5 、コンデンサ上部電極7 のパターンは誘電体層6 よりも小さくならないパターンにて形成し、膜厚は15 μmとした。次に前記第1 のセラミック基板1 上のインダクタ電極2 の形成した面にガラスペースト で接着ガラス層8 のパターンをスクリーン印刷で形成し、５００℃、３０分で脱バインダを行った。そして接着ガラス層8 を挟んで、第1 のセラミック基板1 、第2 のセラミック基板4 を張り合わせ、基板をピーク温度６００℃、１０分保持で焼成を行い、第1 のセラミック基板1 、第2 のセラミック基板4 を接着する。なお第2 のセラミック基板4 はコンデンサ形成面をガラス層側に向けている。焼成の終了した後、基板を個片に切断し、側面に外部電極( 図示せず) を形成することで固体複合部品となり、第1 、第2 のセラミック基板1 ，４を用いることにより特性がよく、しかもこれらのセラミック基板1 ，４は熱膨張係数を合わせているため寸法精度がよく、かつ製造工程が短いものとなる。またインダクタ電極2 の線幅に対する膜厚の比が０．３を越えて膜厚を厚くしたことで、インダクタの性能を良好なものと出来る。また第2 のセラミック基板4 の誘電体層6 を挟み込むコンデンサ導体を、少なくとも焼成後の膜厚を１０μm以上とし、誘電体層6 のパターンサイズよりも小さくならないサイズで形成し、ホウ珪酸鉛からなるガラスフリットを添加していることで、基板、ガラス層、電極自身の誘電体層6 への影響を抑制出来ることとなる。また、前記第1 のセラミック基板1 と前記第2 のセラミック基板4 を接着するための接着ガラス層8 は、接着前に脱バインダするため、ボイドが発生しづらい。以上のことより、信頼性が高い、固体複合部品の製造方法を提供できる。

【００４７】( 実施の形態2 ) 以下に、本発明の電子部品の製造方法の一例の固体複合部品の製造方法について、図面を参照しながら説明する。

【００４８】図2 において固体複合部品の構造図を示すと、( ａ ) にはフェライト 基板の断面図を示す。( ｂ ) には個片にした時の渦巻状導体パターンであるインダクタ電極平面図を示す。( ｃ ) には個片にした時のフェライト 層上のリング状電極平面図を示す。( ｄ ) にはフォルステライト 基板の断面図を示す。( ｅ ) にはフェライト 基板、フォルステライト 基板を張り合わせた時の断面図を示す。( ｆ ) には分割した基板断面図を示す。先ずフェライト 基板１１上にインダクタ電極１２を形成し、その上にフェライト 層１３を形成し、その上にリング状電極１４を形成する。フォルステライト 基板１５上にガラス層１６、コンデンサ下部電極１７、誘電体層１８、コンデンサ上部電極１９からなるコンデンサを形成し、フェライト 基板１１、フォルステライト 基板１５を接着ガラス層２０を挟んで接着し、その後個片に切断している。

【００４９】以下に製造方法を説明する。フェライト 基板１１上に、凹版転写にて銀・パラジウムのペースト を使用してインダクタ電極１２のパターンを形成し、パターン形成を行った基板をピーク温度８５０℃、１０分保持で焼成を行い、インダクタ電極１２を形成した。この時インダクタ電極１２の線幅に対する膜厚の比は０．８とした。前記インダクタ電極１２を形成した上にフェライト ペースト を用いてフェライト 層１３のパターンをスクリーン印刷で形成し、９５０℃、３時間で焼成を行いフェライト 層１３を形成する。前記フェライト 層１３上に、銀・パラジウムのペースト を使用してスクリーン印刷でリング状電極１４のパターンを形成し、パターン形成を行った基板をピーク温度８５０℃、１０分保持で焼成を行い、リング状電極１４を形成した。次に、前記フェライト 基板１１とほぼ同じ熱膨脹係数を持つフォルステライト 基板１５上に、ホウ珪酸チタンからなるガラスペースト を用いてガラス層１６のパターンをスクリーン印刷で形成を行い、ピーク温度９００℃、１０分キープで焼成を行いガラス層１６を形成する。そしてガラス層１６上にホウ珪酸アルミニウムからなるガラスフリットを添加した銀・パラジウムペースト でコンデンサ下部電極１７のパターンをスクリーン印刷で形成し、コンデンサ下部電極１７上に誘電体ペースト を使用して誘電体層１８のパターンをスクリーン印刷で形成を行い、誘電体層１８上に下部電極に用いた銀・パラジウムペースト によりコンデンサ上部電極１９のパターンをスクリーン印刷で形成する。この基板をピーク温度８５０℃、１０分キープで焼成を行いコンデンサを形成する。この時コンデンサ下部電極１７、コンデンサ上部電極１９のパターンは誘電体層１８よりも小さくならないパターンにて形成し、膜厚は２０μmとした。次にフェライト 基板１１上のインダクタ電極１２の形成した面と、フォルステライト 基板１５のコンデンサを形成した面にガラスペースト で接着ガラス層２０のパターンをスクリーン印刷で形成し、５００℃、３０分で脱バインダを行った。そして接着ガラス層２０を挟んでフェライト 基板１１、フォルステライト 基板１５を張り合わせ、基板をピーク温度７００℃、１０分保持で焼成を行い、フェライト 基板１１、フォルステライト 基板１５を接着する。焼成の終了した後、基板を個片に切断し、側面に外部電極( 図示ず) を形成することで固体複合部品となり、基板１１，１５は熱膨脹係数を合わせているため寸法精度がよいものとなる。またインダクタ電極１２の線幅に対する膜厚の比が０．３を越えて膜厚を厚くし、パターン間に非磁性材料を形成し、インダクタ電極１２上にリング状電極１４を形成したことで、１つの部品中にインダクタ電極１４を複数個形成してもインダクタの性能を良好なものとすることが出来る。またコンデンサの下にホウ珪酸チタンからなるガラス層１６を形成し、誘電体層１８を挟

み込むコンデンサ導体を、膜厚を１０μｍ以上とし、誘電体層１８のパターンサイズよりも小さくならないサイズで形成し、ホウ珪酸アルミニウムからなるガラスフリットを添加していることで、基板、ガラス層、電極自身の誘電体層１８への影響を抑制出来ることとなる。また、前記フェライト基板１１と前記フォルステライト基板１５を接着するためのガラス層１６は、接着前に脱バインダするため、ボイドが発生しづらい。以上のことより、信頼性が高い、固体複合部品の製造方法を提供できる。

【００５０】（実施の形態３）以下に、本発明の電子部品の製造方法の一例の固体複合部品の製造方法について、図面を参照しながら説明する。

【００５１】図3において固体複合部品の構造図を示すと、（ａ）にはフェライト基板の断面図を示す。（ｂ）には個片にした時の渦巻状導体パターンであるインダクタ電極平面図を示す。（ｃ）には貫通孔を形成したフォルステライト基板の平面図を示す。（ｄ）にはフォルステライト基板の断面図を示す。（ｅ）にはフェライト基板、フォルステライト基板を張り合わせた時の断面図を示す。（ｆ）には分割した基板断面図を示す。先ず、フェライト基板２１上に非磁性ガラス層２２とインダクタ電極２３を形成し、これらの上にフェライト層２４を形成する。フォルステライト基板２５に貫通孔２６を形成した後、前記フォルステライト基板２５上にコンデンサ下部電極２７、誘電体層２８、コンデンサ上部電極２９からなるコンデンサを形成し、フェライト基板２１、フォルステライト基板２５を接着ガラス層３０を挟んで接着し、個片に切断している。

【００５２】以下に製造方法を説明する。フェライト基板２１上に溝を形成、この溝にガラスペーストを用いて非磁性ガラス層２２のパターンをスクリーン印刷で形成を行い、ピーク温度９００℃、１０分で焼成を行いガラス層２２を形成する。そして凹版転写によって銀・パラジウムのペーストを使用してインダクタ電極２３のパターンを形成し、パターン形成を行った基板をピーク温度８５０℃、１０分保持で焼成を行い、インダクタ電極２３を形成した。この時インダクタ電極２３の線幅に対する膜厚の比は１．５とした。前記インダクタ電極２３を形成した上にフェライトペーストを用いてフェライト層２４のパターンをスクリーン印刷で形成し、９５０℃、３時間で焼成を行いフェライト層２４を形成する。次に、前記フェライト基板２１とほぼ同じ熱膨脹係数を持つ、貫通孔２６を形成したフォルステライト基板２５上に、ホウ珪酸カルシウムからなるガラスフリットを添加した銀・白金ペーストでコンデンサ下部電極２７のパターンをスクリーン印刷で形成し、コンデンサ下部電極２７上に誘電体ペーストを使用して誘電体層２８のパターンをスクリーン印刷で形成し、誘電体層２８上にコンデンサ下部電極２７で用いた銀・白金ペーストによりコンデンサ上部電極２９のパターンをスクリーン印刷で形成する。この基板をピーク温度９００℃、１０分キープで焼成を行いコンデンサを形成する。この時コンデンサ下部電極２７、コンデンサ上部電極２９のパターンは誘電体層２８よりも小さくならないパターンにて形成し、膜厚は１３μｍとした。次にフェライト基板２１上のインダクタ電極２３を形成した面と、フォルステライト基板２５のコンデンサを形成した面にガラスペーストで接着ガラス層３０のパターンをスクリーン印刷で形成し、５００℃、３０分で脱バインダを行った。そして接着ガラス層３０を挟んでフェライト基板２１、フォルステライト基板２５を張り合わせ、基板をピーク温度６８０℃、１０分保持で焼成を行い、フェライト基板１、フォルステライト基板２５を接着する。焼成の終了した後、基板を個片に切断し、側面に外部電極（図示せず）を形成することで固体複合部品となり、フェライト基板２１とフォルステライト基板２５は熱膨脹係数を合わせているため寸法精度がよいものとなる。またインダクタ電極２３の線幅に対する膜厚の比が０．３を越えて膜厚を厚くし、パターン間の溝に非磁性材料であるガラス層を形成したことで、１つの部品中にインダクタ電極２３を複数個形成してもインダクタの性能を良好なものとすることが出来る。また誘電体層２８を挟み込むコンデンサ導体を、膜厚を１０μｍ以上とし、誘電体層２８のパターンサイズよりも小さくならないサイズで形成し、ホウ珪酸カルシウムからなるガラスフリットを添加していることで、基板、ガラス層、電極自身の誘電体層２８への影響を抑制出来ることとなる。また、前記フェライト基板２１と前記フォルステライト基板２５を接着するための接着ガラス層３０は、フォルステライト基板２５にあらかじめ貫通孔２６を形成したことで、接着層の焼成時、発生するガスが貫通孔２６へ抜けるため、細かいボイドも発生せず、より高い信頼性を得られるものとなる。以上のことより、信頼性が高い、固体複合部品の製造方法を提供できる。

【００５３】（実施の形態４）以下に、本発明の電子部品の製造方法の一例の固体複合部品の製造方法について、図面を参照しながら説明する。

【００５４】図4において固体複合部品の構造図を示すと、（ａ）にはフェライト基板の断面図を示す。（ｂ）には個片にした時の渦巻状導体パターンであるインダクタ電極平面図を示す。（ｃ）にはフォルステライト基板の断面図を示す。（ｄ）にはフェライト基板、フォルステライト基板を張り合わせた時の断面図を示す。（ｅ）には分割した基板断面図を示す。先ず、フェライト基板３１上にインダクタ電極３２とリング状電極３３、非磁性ガラス層３４を形成し、これらの上にフェライト層３５を形成する。フォルステライト基板３６上にガラス層３７を形成し、前記ガラス層３７上にコンデンサ下部電極３８、誘電体層３９、コンデンサ上部電極４０からな

るコンデンサを形成し、フェライト基板３１、フォルステライト基板３６を接着ガラス層４１を挟んで接着し、個片に切断している。

【００５５】以下に製造方法を説明する。フェライト基板３１上に凹版転写によって銀のペーストを使用してインダクタ電極３２とリング状電極３３のパターンを形成し、パターン形成を行った基板をピーク温度９００℃、１０分保持で焼成を行い、インダクタ電極３２とリング状電極３３を形成した。この時インダクタ電極３２の線幅に対する膜厚の比は１．５とした。また、前記リング状電極３３はビアにより接続されている（図示せず）。前記電極を形成した基板上にガラスペーストを用いて非磁性ガラス層３４のパターンをスクリーン印刷で形成を行い、ピーク温度９００℃、１０分で焼成を行いガラス層３４を形成する。前記インダクタ電極３２を形成した上にフェライトペーストを用いてフェライト層３５のパターンをスクリーン印刷で形成し、９７０℃、３時間で焼成を行いフェライト層３５を形成する。次に、前記フェライト基板３１とほぼ同じ熱膨脹係数を持つフォルステライト基板３６上に、ホウ珪酸ガラスのペーストを用いてガラス層３７のパターンをスクリーン印刷で形成を行い、ピーク温度９００℃、１０分キープで焼成を行いガラス層３７を形成する。そしてガラス層３７上にホウ珪酸チタンからなるガラスフリットを添加した銀・白金ペーストでコンデンサ下部電極３８のパターンをスクリーン印刷で形成し、コンデンサ下部電極３８上に誘電体ペーストを使用して誘電体層３９のパターンをスクリーン印刷で形成し、誘電体層３９上にコンデンサ下部電極３８で用いた銀・白金ペーストによりコンデンサ上部電極４０のパターンをスクリーン印刷で形成する。この基板をピーク温度９００℃、１０分キープで焼成を行いコンデンサを形成する。この時コンデンサ下部電極３８、コンデンサ上部電極４０のパターンは誘電体層３９よりも小さくならないパターンにて形成し、膜厚は１３μｍとした。次にフェライト基板３１上のインダクタ電極３２を形成した面と、フォルステライト基板３６のコンデンサを形成した面にガラスペーストで接着ガラス層４１のパターンをスクリーン印刷で形成し、５００℃、３０分で脱バインダを行った。そして接着ガラス層４１を挟んでフェライト基板３１、フォルステライト基板３６を張り合わせ、基板をピーク温度７３０℃、１０分保持で焼成を行い、フェライト基板３１、フォルステライト基板３６を接着する。焼成の終了した後、基板を個片に切断し、側面に外部電極（図示せず）を形成することで固体複合部品となる。

【００５６】なお、基板３１，３６は熱膨脹係数を合わせているため寸法精度がよいものとなる。またインダクタ電極３２の線幅に対する膜厚の比が０．３を越えて膜厚を厚くし、パターン間に非磁性材料であるガラス層を形成し、インダクタ電極３２周辺にリング状電極３３を形成したことで、１つの部品中にインダクタ電極３２を複数個形成してもインダクタの性能を良好なものとすることが出来る。またコンデンサの下にホウ珪酸ガラス層３７を形成し、誘電体層３９を挟み込むコンデンサ導体を、膜厚を１０μｍ以上とし、誘電体層３９のパターンサイズよりも小さくならないサイズで形成し、ホウ珪酸チタンからなるガラスフリットを添加していることで、基板、ガラス層、電極自身の誘電体層３９への影響を抑制出来ることとなる。以上のことより、信頼性が高い、固体複合部品の製造方法を提供できる。

【００５７】なお、以上の説明では4つの実施の形態の例で説明したが、その他熱膨脹係数をほぼ同じくする電極配線を必要とするような配線基板においても同様に実施可能である。さらに、上記実施形態では、渦巻状導体パターンは単層のもので行っているが、複数層に形成しても同様の固体複合部品が得られるものである。また渦巻状導体パターンは、インダクタ電極として使用できる構成の配線電極パターンであるならば、同様に実施可能である。

【００５８】また第1、第2のセラミック基板を接着層により接合した後に少なくとも一方を研削し基板厚みを薄くしても同様の固体複合部品が得られるものである。コンデンサ導体に使用するガラスフリットに4種類のもので説明しているが、ホウ珪酸、ホウ珪酸鉛、ホウ珪酸カルシウム、ホウ珪酸アルミニウム、ホウ珪酸チタンのいずれか、もしくは混合物、もしくは化合物からなるガラスフリットであるならば同様の効果が得られるものである。またコンデンサの下に形成するガラス層は2種類のもので説明しているが、ホウ珪酸、ホウ珪酸鉛、ホウ珪酸カルシウム、ホウ珪酸アルミニウム、ホウ珪酸チタンのいずれか、もしくは混合物、もしくは化合物からなるガラスフリットであるならば同様の効果が得られるものである。

【００５９】

【発明の効果】以上のように本発明によれば、インダクタ層およびコンデンサ層はセラミック基板上に形成するので、特性向上を図ることができる。

【００６０】さらに、第1のセラミック基板および第2のセラミック基板は、未焼成のセラミック基板である第1の未焼成セラミック基板および第2の未焼成セラミック基板を焼成して形成しているので、張合体を焼成して焼成体を形成する際に、第1のセラミック基板および第2のセラミック基板が、全体的に熱収縮することがない。これにより、第1、第2のセラミック基板上に形成したインダクタ層およびコンデンサ層が、第1、第2のセラミック基板の収縮に合わせて、収縮してしまうことがなく、寸法精度を向上させることができるとともに、後工程等において、寸法を調整する必要もなく、製造工程を簡略化することもできる。

【００６１】この結果、特性向上および寸法精度の向上

を図った固体複合部品の製造方法を提供することができるものである。

【図面の簡単な説明】

【図1】（a）は本発明の一実施の形態の固体複合部品の製造方法における第1のセラミック基板の構造を示す断面図

（b）は同第1のセラミック基板上の個片にした時のインダクタ電極パターンの平面図

（c）は同第2のセラミック基板の構造を示す断面図

（d）は同第1のセラミック基板と第2のセラミック基板を接着層を介して一体化したときの断面図

（e）は同固体複合部品を切断した時の断面図

【図2】（a）は本発明の他の実施の形態の固体複合部品の製造方法におけるフェライト基板の構造を示す断面図

（b）は同フェライト基板上の個片にした時のインダクタ電極パターンの平面図

（c）は同フェライト基板のフェライト層状のリング状電極パターンの平面図

（d）は同フォルステライト基板の構造を示す断面図

（e）は同フェライト基板とフォルステライト基板を接着層を介して一体化したときの断面図

（f）は同固体複合部品を切断した時の断面図

【図3】（a）は本発明のさらに他の実施の形態の固体複合部品の製造方法におけるフェライト基板の構造を示す断面図

（b）は同フェライト基板上の個片にした時のインダクタ電極パターンの平面図

（c）は同貫通孔を形成したフォルステライト基板の平面図

（d）は同フォルステライト基板の構造を示す断面図

（e）は同フェライト基板とフォルステライト基板を接着層を介して一体化したときの断面図

（f）は同固体複合部品を切断した時の断面図

【図4】（a）は本発明の一実施の形態の固体複合部品の製造方法におけるフェライト基板の構造を示す断面図

（b）は同フェライト基板上の個片にした時のインダクタ電極パターンの平面図

（c）は同フォルステライト基板の構造を示す断面図

（d）は同フェライト基板とフォルステライト基板を接着層を介して一体化したときの断面図

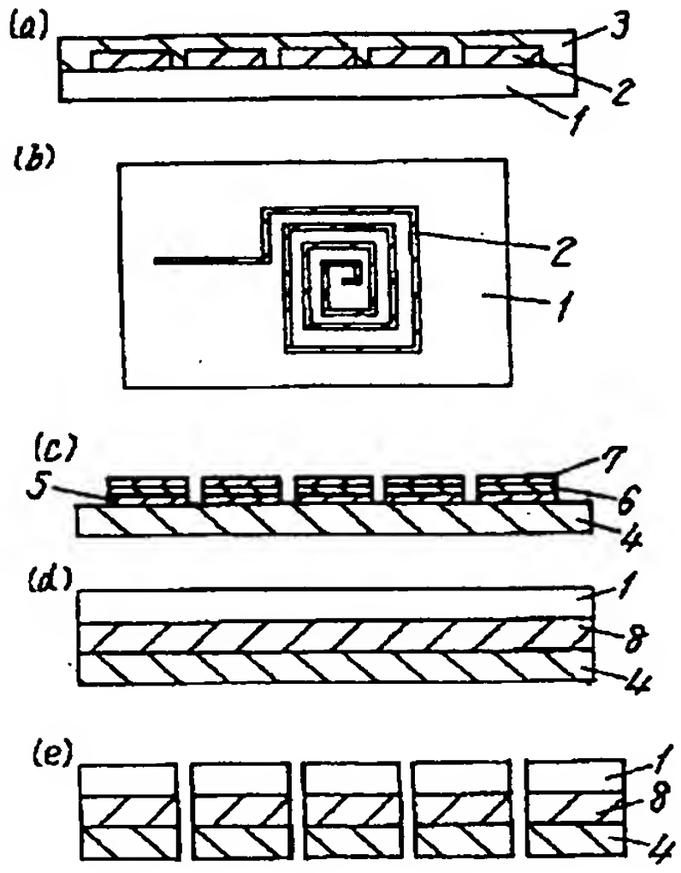
（e）は同固体複合部品を切断した時の断面図

【符号の説明】

1　第1のセラミック基板
2　インダクタ電極
3　フェライト層
4　第2のセラミック基板
5　コンデンサ下部電極
6　誘電体層
7　コンデンサ上部電極
8　接着ガラス層
11　フェライト基板
12　インダクタ電極
13　フェライト層
14　リング状電極
15　フォルステライト基板
16　ガラス層
17　コンデンサ下部電極
18　誘電体層
19　コンデンサ上部電極
20　接着ガラス層
21　フェライト基板
22　非磁性ガラス層
23　インダクタ電極
24　フェライト層
25　フォルステライト基板
26　貫通孔
27　コンデンサ下部電極
28　誘電体層
29　コンデンサ上部電極
30　接着ガラス層
31　フェライト基板
32　インダクタ電極
33　リング状電極
34　非磁性ガラス層
35　フェライト層
36　フォルステライト基板
37　ガラス層
38　コンデンサ下部電極
39　誘電体層
40　コンデンサ上部電極
41　接着ガラス層

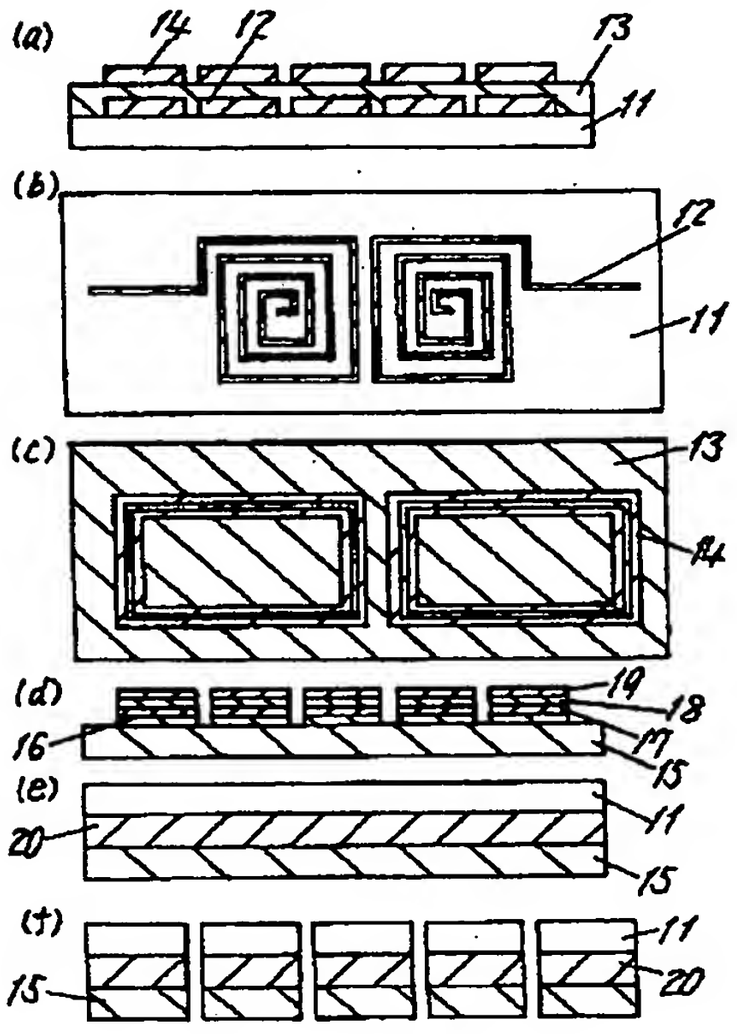
【図1】

1 第1のセラミック基板　5 コンデンサ下部電極
2 インダクタ電極　6 誘電体層
3 フェライト層　7 コンデンサ上部電極
4 第2のセラミック基板　8 接着ガラス層



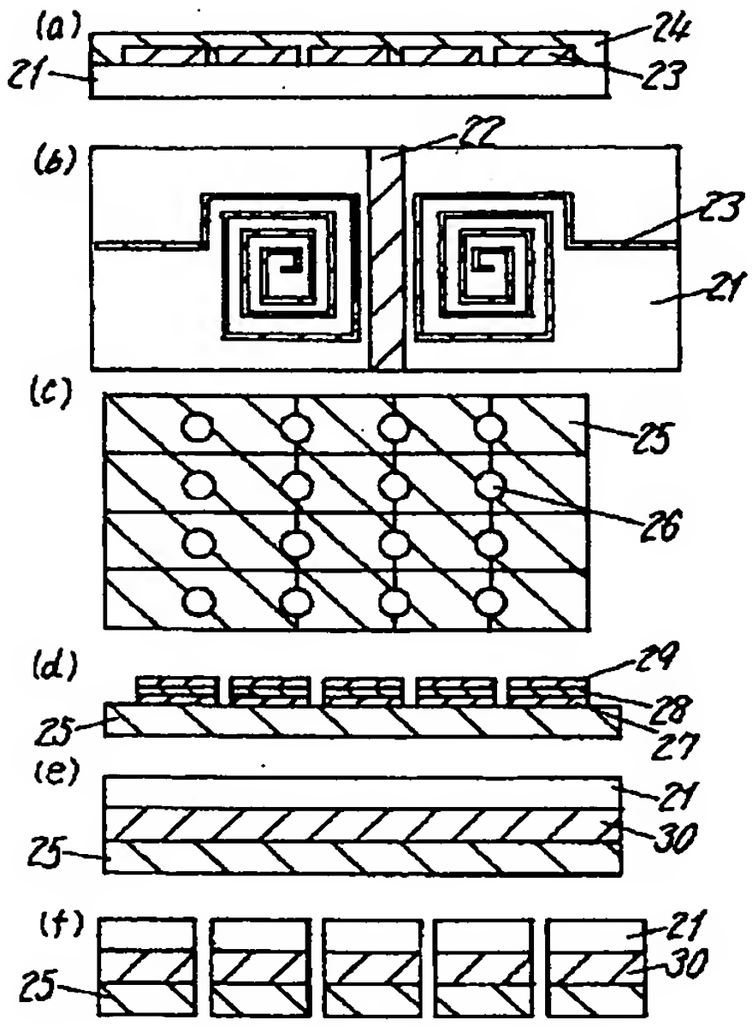

【図2】

11 フェライト基板　16 ガラス層
12 インダクタ電極　17 コンデンサ下部電極
13 フェライト層　18 誘電体層
14 リング状電極　19 コンデンサ上部電極
15 フォルステライト基板　20 接着ガラス層



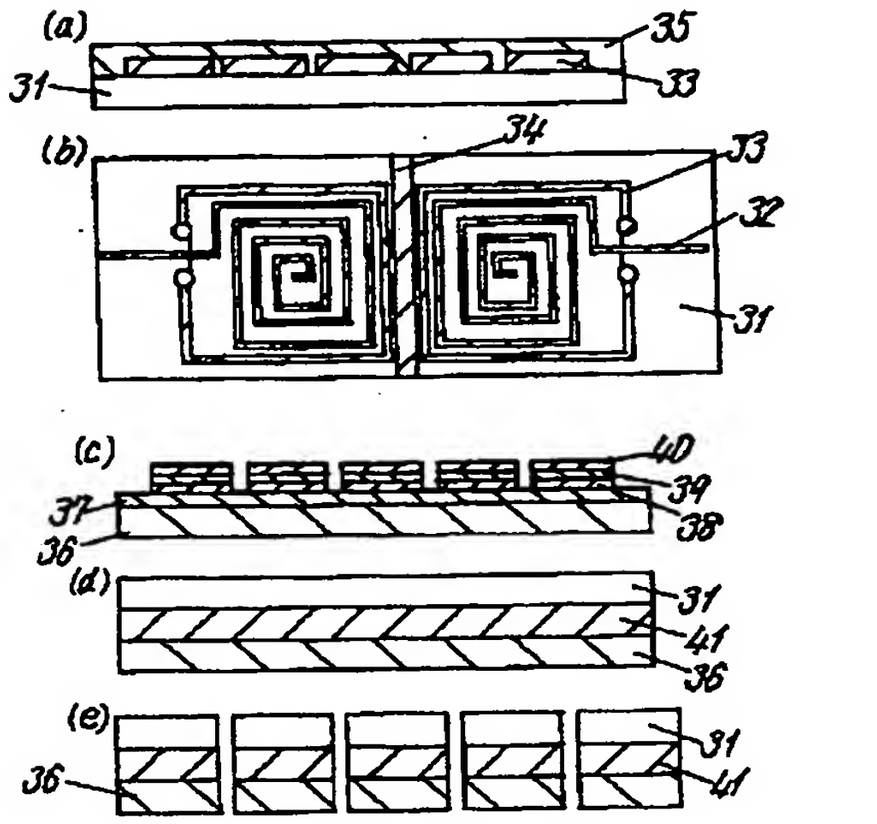
【図3】

21 フェライト基板
22 非磁性ガラス層
23 インダクタ電極
24 フェライト層
25 フォルステライト基板
26 貫通孔
27 コンデンサ下部電極
28 誘電体層
29 コンデンサ上部電極
30 接着ガラス層




【図4】

31 フェライト基板
32 インダクタ電極
33 リング状電極
34 非磁性ガラス層
35 フェライト層
36 フォルステライト基板
37 ガラス層
38 コンデンサ下部電極
39 誘電体層
40 コンデンサ上部電極
41 接着ガラス層

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